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Minicomputer-linked work station eases large-project management/127

Streaming-tape drive shrinks to 5¼-in. disk-drive size/147

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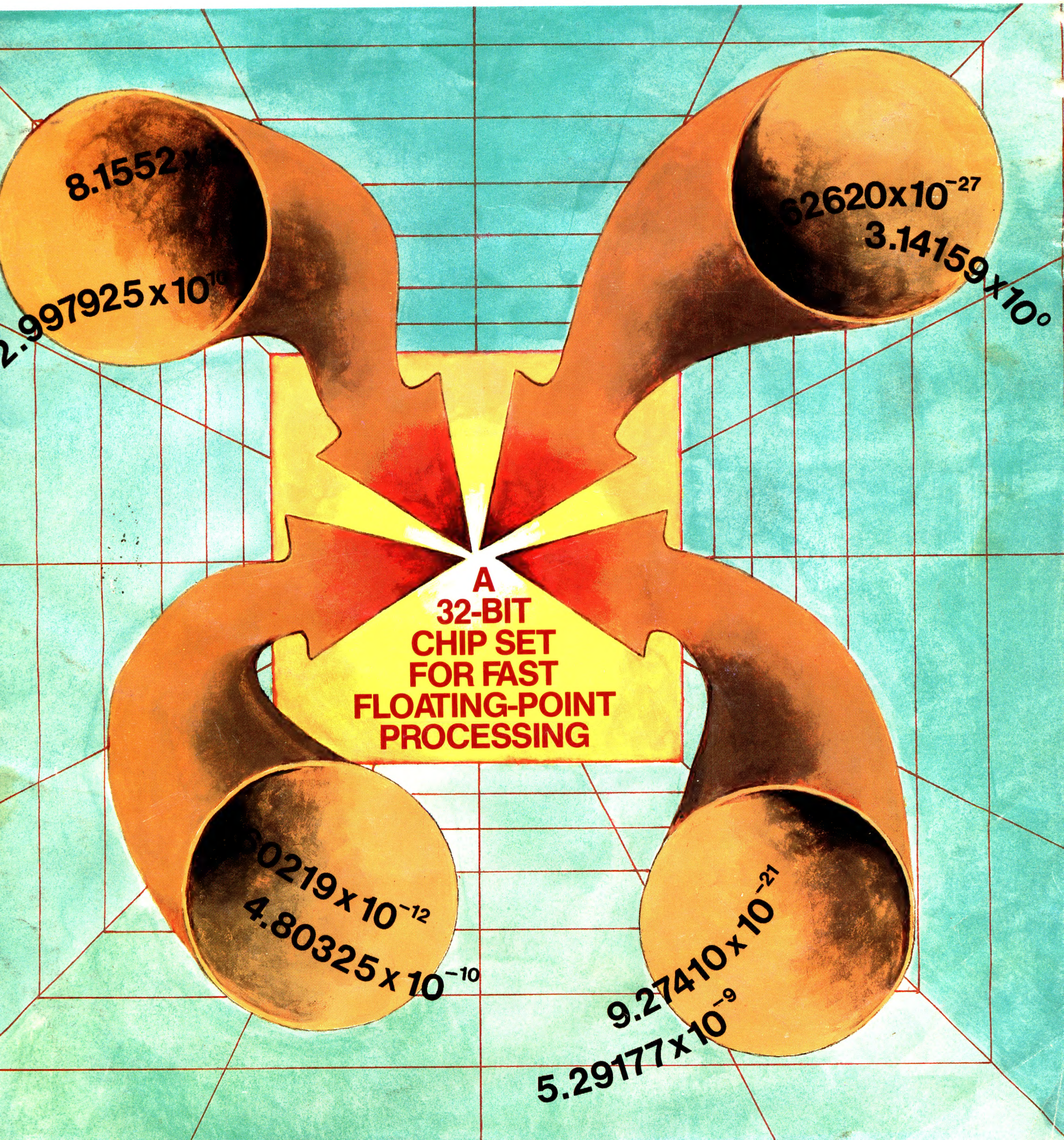

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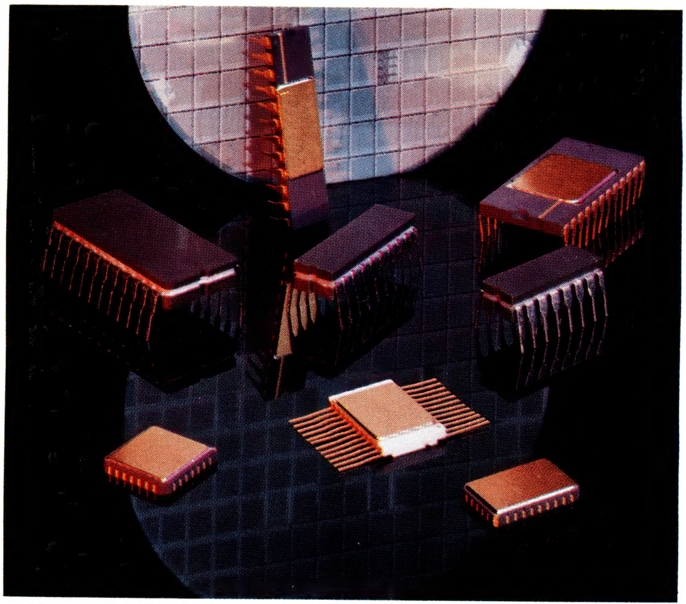

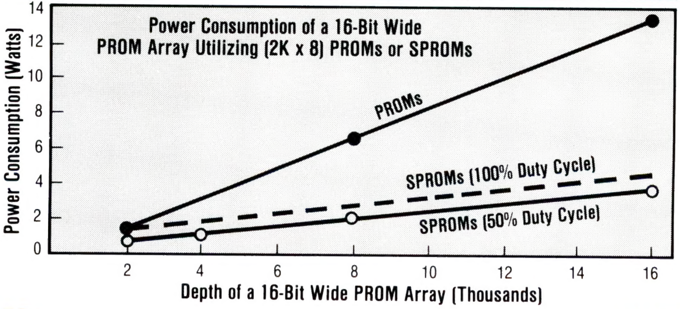
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4
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29681A	16K	2048 x 8	50	180
29651	8K	2048 x 4	70	170
29651A	8K	2048 x 4	60	170
29631	8K	1024 x 8	70	170
29631A	8K	1024 x 8	50	170
29621	4K	512 x 8	65	155
29611	2K	512 x 4	55	130

SPROMs

Part Number	Density	Organization	Speed T_{AA} (nS)	Power I_{CC} (mA)*
29673	32K	4096 x 8	85	55
29683	16K	2048 x 8	85	50
29683A	16K	2048 x 8	50	50
29653	8K	2048 x 4	75	45
29653A	8K	2048 x 4	65	45
29633	8K	1024 x 8	70	45
29633A	8K	1024 x 8	50	45
29623	4K	512 x 8	70	45
29613	2K	512 x 4	60	45

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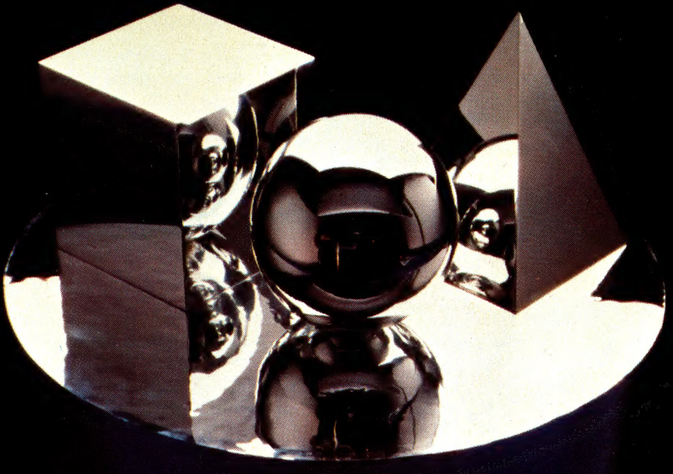

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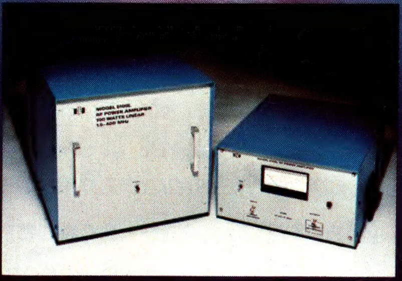

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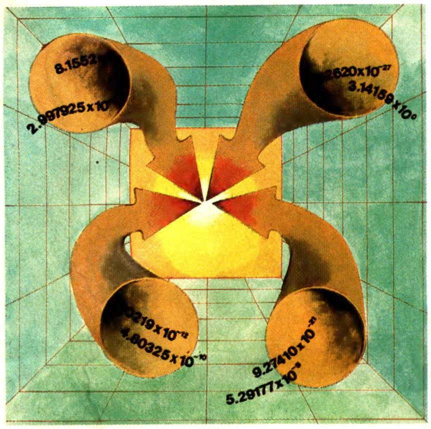

Cover illustrated by Art Director Fred Sklenar.

Cover Story

Two chips set floating-point speed record, 121

Their 5-megahertz throughput rate for IEEE-format 32-bit floating-point operations sets the pace for dedicated number-crunching systems that need real-time math capability.

Major New Developments

Standard cells become semicustom processors

Standard-cell–based design houses are aiming their single-chip systems at high-volume consumer markets, and even the smallest of these companies will get a shot at the business. That's the word from the Custom IC Conference, 93

Zinc oxide on MOS yields one-chip microphone

A single chip contains a thin-film acoustic sensor fabricated atop C-MOS signal-conditioning and -amplifying circuitry, 48

Logic design system manages team projects

A VAX minicomputer helps computer-aided–design work stations and office terminals automate not only very large-scale integrated-circuit design efforts but their documentation and management as well, 127

Shallower tape drives for mass-storage backup

A quarter-inch streaming tape drive moves to back up Winchester drives in small systems quickly and cheaply while keeping the storage media removable, 147

Electron-beam scanning for real-time SAW images

A system using an electron beam as a noncontact probe with phase-synchronous pulsing re-creates surface-acoustic-wave patterns on a cathode-ray tube for dynamic testing of existing devices and possible insight into new designs, 132

Aiding Ada programming

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Highlights

Cover: Two chips make up a fast floating-point processor, 121

A pair of chips zoom through 5 million floating-point operations a second, laying the groundwork for high-speed array processors that use the standard single-precision format of the Institute of Electrical and Electronic Engineers. Sharing a common pipelined architecture, one chip is a multiplier and the other is an arithmetic and logic unit.

Battle royal roils the home-computer market, 96

In keeping with the best traditions of the U. S. consumer-electronics market, a real donnybrook is under way among makers of home computers. Price cutting in order to gain market share has reached the state of retail warfare, and competition from powerful new entrants is strengthening. On the other hand, consumers are flocking to buy these inexpensive machines, and the aftermarket for software looks to be a bright spot.

CAE system handles project management, 127

For large-scale team efforts in electronic design, a computer-aided engineering system links work stations to the VAX-11 minicomputer so as to incorporate sophisticated project-management tools, as well as logic-design and analysis aids. Local data bases are kept in step with the central data base, and economical office terminals supplement design work stations.

Scanning electron beam displays SAW images on TV screen, 132

To produce real-time TV images of surface acoustic waves, a scanning electron-beam microscope operates in a stroboscopic voltage-contrast mode. Though there are other SEM techniques, this one best captures SAW high-frequency fields in models of filters, convolvers, and delay lines.

Well-furnished microprocessor is system designer's friend, 143

A 16-bit microprocessor that incorporates a host of peripheral functions can radically simplify the process of system design. In support of that claim, this second and final article on the chip examines the design of a personal work station for business use.

Streaming-tape drive challenges floppies as hard-disk backup, 147

Pared down to fighting trim, a ¼-inch streaming tape drive has the form factor of a half-height 5¼-in. 1-megabyte floppy-disk drive, yet can hold 60 times as much data. Thus it is a strong competitor for the role of backup in Winchester hard-disk systems.

Coming up . . .

The changing world of the electronics engineer, an in-depth look . . . incorporating increased functional checks in a tester designed for very large-scale integrated circuits.

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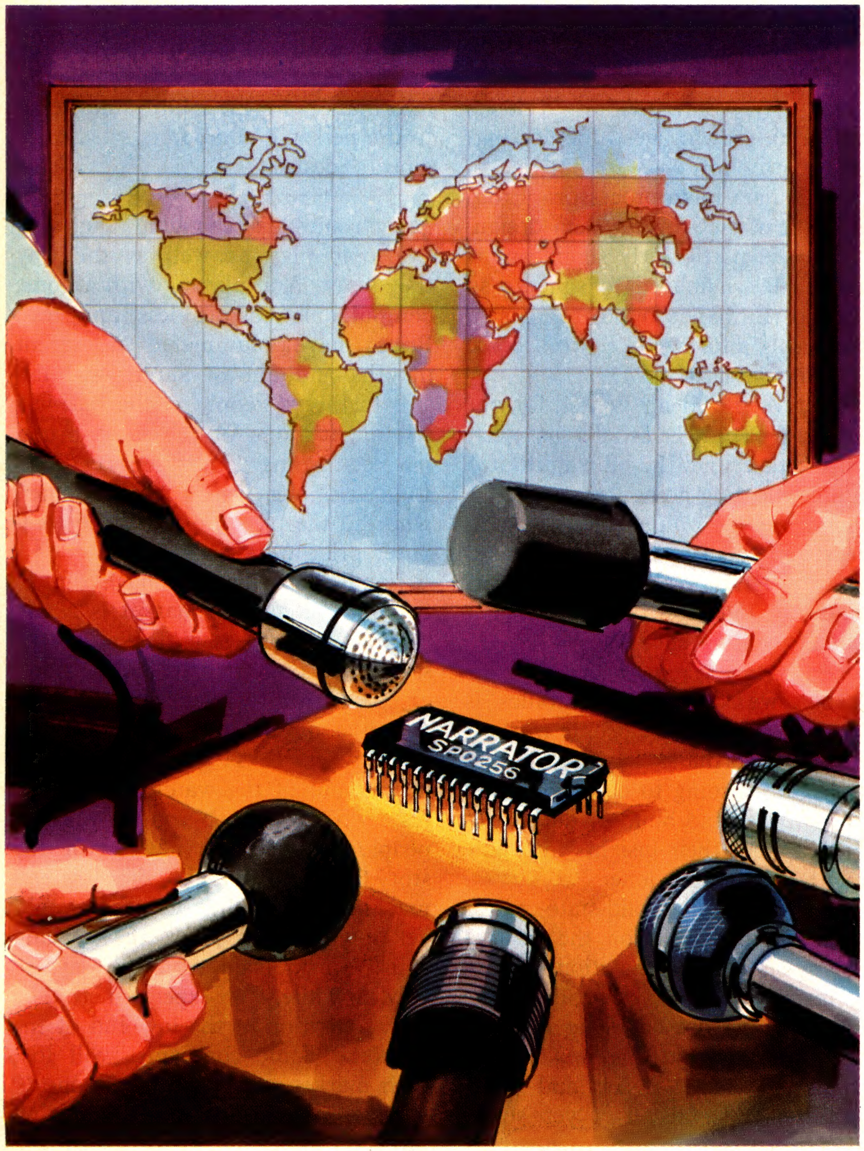

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Publisher's letter

On a swing to New York last November, the top brass of Weitek Corp., a 2½-year-old Silicon Valley outfit, stopped by to tell editor-in-chief Sam Weber and microsystems editor Steve Evanczuk about an impressive new chip set.

"We hear about all sorts of dedicated chips for all sorts of applications," says Steve, "but Weitek's chips fill a growing need for floating-point math chips that are not tied to a particular microprocessor. From the point of view of a system designer, what is particularly significant is that Weitek managed to squeeze so much performance out of a pair of chips using a format likely to become an IEEE standard."

So Steve signed up Weitek for our cover story (p. 121). It tells just what it takes to crunch 32-bit values at 5 million floating-point operations a second, all the while conforming to the requirements of the Institute of Electrical and Electronics Engineers standard 754 for single-precision floating-point calculations.

When we say that electronics is changing the way people work, it is really shorthand for saying that people are turning to computers and new software and building data bases to implement their insights into how people get the job done.

Early last fall, solid-state editor Rod Beresford went on the trail of the engineering work station, doubly significant because it changes the way engineers are changing the way the rest of us work [*Electronics,* Nov. 17, 1982, p. 123]. "I saw, and I was impressed," he recalls, "yet something was missing."

That something surfaced during a lunch Rod had with Steve Shopbach, marketing vice president of Cadtec Corp. "He pointed out that on-line design can change not only the way designs are done, but also the way designers are managed," remembers Rod. "The idea was that complexity extends all the way from chips and boards to the interactions among the many people that contribute to it." Cadtec's labors to address those further complexities have now borne their first fruit (see "Logic design system manages team projects," p. 127). "Their [Cadtec's] approach is probably the first of many difficult steps in the maturation of design automation," notes Rod. "When the big semiconductor and systems houses say they're building an integrated design system, they really mean integrated—from the corporate information-system mainframe down to the personal computers on the engineers' desks."

Electronics is changing the way people play as well as the way they work. And playing with a home computer is costing less and less. Prices have plummeted in recent months and almost surely will fall still further. "People in the business tell me it's one of the most brutal markets going on," reports Rob Lineback, our Dallas bureau chief, who did the piece on the home-computer price wars (p. 93).

For Rob, the current maelstrom in the home-computer market is a tale retold. "It looks as if they're on the same road that watches and consumer calculators traveled," he says. As a native of Dallas, he was on the scene when Texas Instruments went in and out of the watch business in just two years. Rob routinely asked people he was interviewing for the story if they thought the low-end machines now selling for $100 would get down to $50 before the slashing ends. "No one said 'no,' " he says.

Meanwhile, Rob expects there'll be heavy attrition at the low end of the market. "Some companies will lose their market share and their money," he says. Others, he thinks, may find salvation in the market niche just under $1,200 or so, where systems with floppy disks start. And unlike watches and consumer calculators, he says, there may be enough of an aftermarket in software that companies selling computers consoles as loss leaders may still eke out a profit.

Paul W

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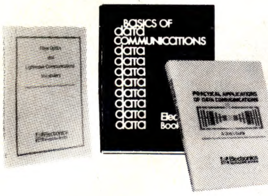
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Readers' comments

The politics of concern

To the Editor: Ray Connolly's account of the recent hearings before the House Judiciary Subcommittee on Immigration, Refugees, and International Law held on March 10 ("IEEE talks tough on foreign EE grads," March 24, p. 54) was lacking in certain important elements.

In the first place, I was not supporting the presentation by the Institute of Electrical and Electronics Engineers, as the story states. Indeed, I appeared as a separate witness representing the Committee of Concerned EEs. Further, Connolly's distorted account ignored what was perhaps the most important element of the hearings to American working engineers—that, for the first time, we working engineers have forced the the IEEE to reverse its previously stated positions.

Dr. Lewis, who represented not just the IEEE but the umbrella organization, the American Association of Engineering Societies, not only strongly urged that a "return home" provision be added to the pending Immigration Reform and Control Act but also clearly stated that the survey demonstrating shortages of computer and electronics engineers that was produced by the employer-dominated American Electronics Association was fatally flawed.

I also pointed out to the subcommittee the many flaws in the survey conducted by the AEA. These include the perhaps intentionally ambiguous wording of the questions and the reply sheet and, more obvious, the faulty method of obtaining the data. For example, since many competing employers of engineers in the Air Force fighter plane industry were asked for projections of the number of additional engineers needed in 1985, the sum of the replies yielded large errors. This is because each such employer will base its reply on the expectation that it will receive the contract. The reality is that the contract, if it is awarded at all, will go to only one of them.

These flaws have been clear from the day the AEA issued its projections. Yet despite this, and despite the fact that the readers of *Electronics* are technically trained people, this magazine has never seen fit to critically examine the methodology of the AEA survey.

Irwin Feerst
Massapequa Park, N. Y.

■ **Senior Editor Connolly replies:** *There never has been any "love affair" between this reporter and the AEA—or any other industry, management, or labor group—as reader Feerst inaccurately alleges. The story in question accurately stated, first, that the position of the Institute of Electrical and Electronics Engineers on deporting alien engineers educated in the U. S. for two years is a new one, "enunciated for the first time" at the congressional hearings and, second, that Feerst's separate testimony supported that view—not a new one for him. The IEEE has not acknowledged that Feerst's splinter group forced that change.*

The many flaws that Feerst sees in the AEA survey are an old story. The challenges to AEA data were first detailed in depth by Electronics *when the association's report was presented in Washington some 18 months ago ("U. S. asked to help produce more EEs," Nov. 17, 1981, p. 96) with a follow-up story in the next issue ("EE shortage divides industry, IEEE," Nov. 30, 1981, p. 43). If reader Feerst has forgotten, the first story began: "Some electronics engineers and computer scientists forced to look for new jobs because of the national economic downturn find it hard to comprehend manufacturers who claim there is a continuing shortage of electronic engineers and computer scientists . . ." I should certainly recall those words; I wrote them.*

The follow-up story, which I also reported, is best summarized by its headline. That story details the pros and cons of the issue, identifying point by point the complaints raised then by IEEE's Bruno Weinschel about the AEA survey. Reporting all sides of an issue accurately and without bias is a first principle of journalism. That is what Electronics *did in this case, has done in the past, and continues to do.*

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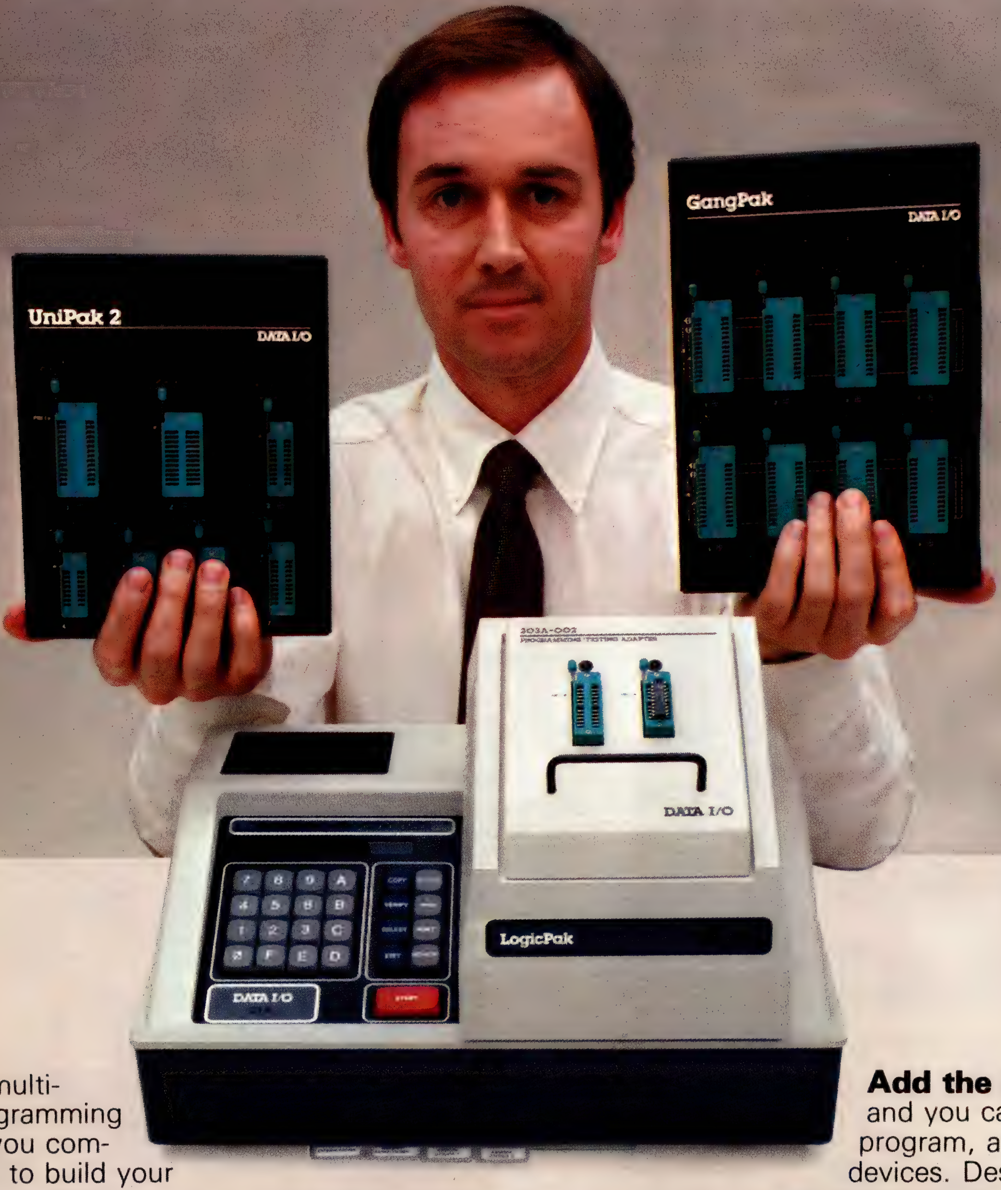

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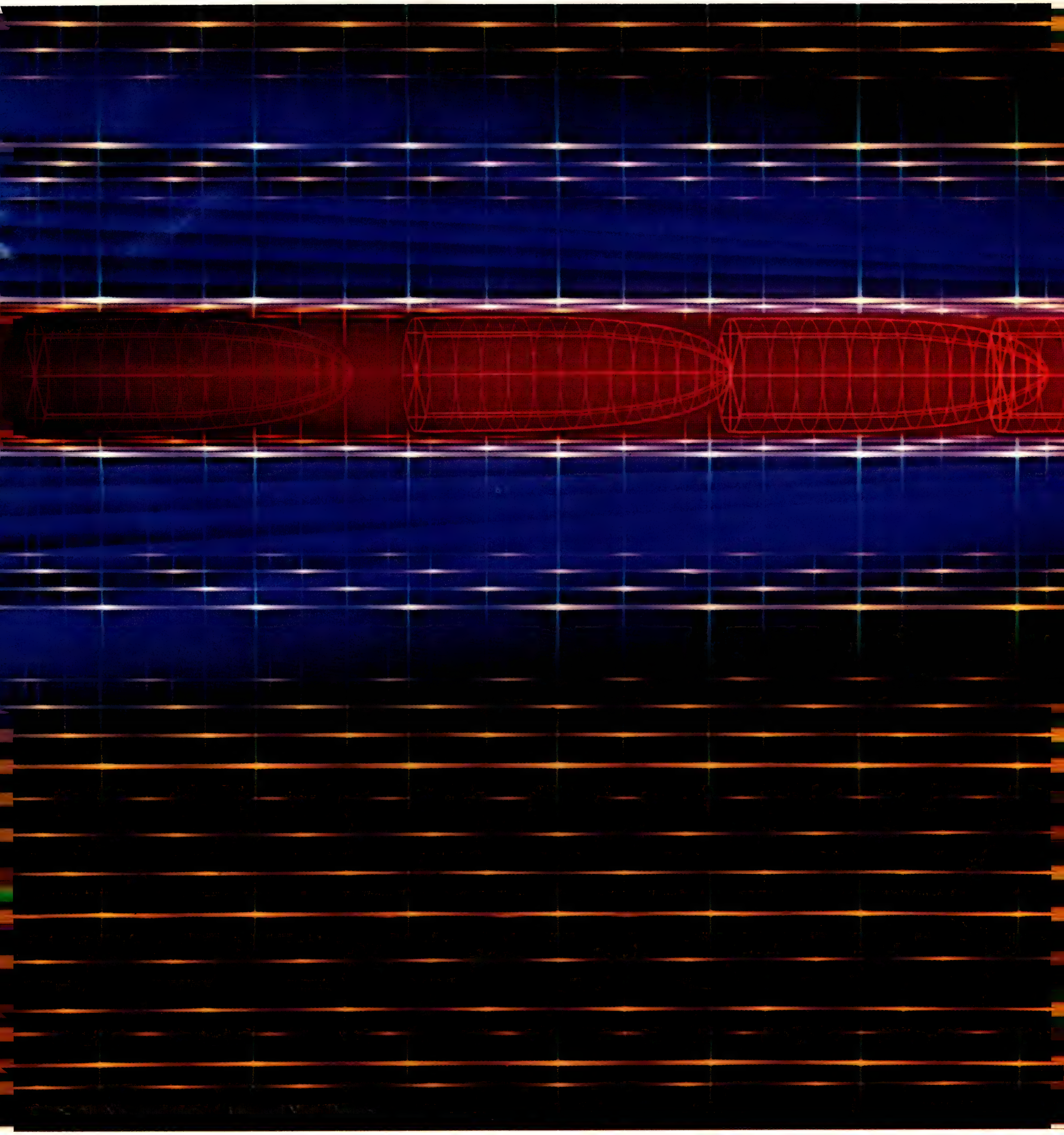

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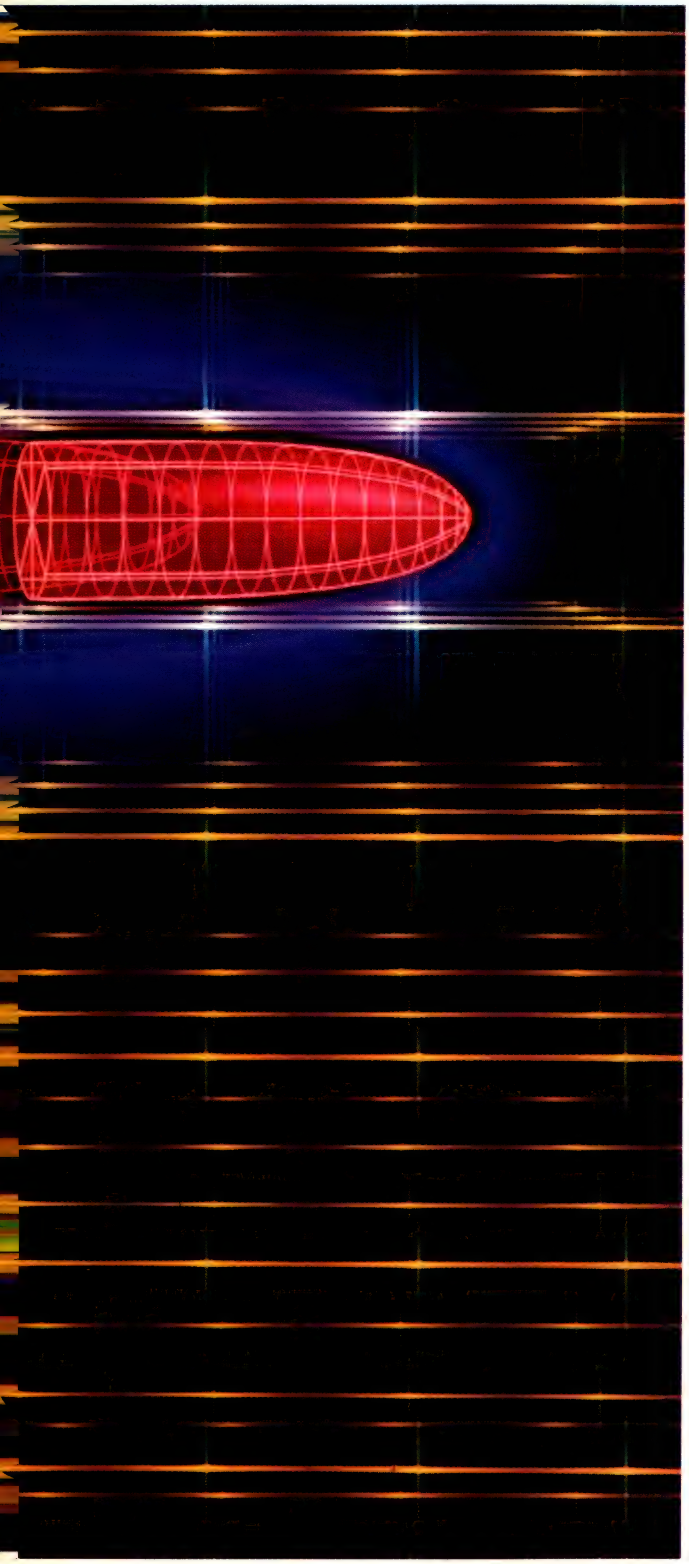

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Turning back the 'rising tide of mediocrity'

Now the U. S. has reports from two blue-ribbon panels urging that it get its educational house in order. First, "An Open Letter to the American Public" was issued by an 18-member Federal study group, the National Commission on Excellence in Education. That body warns: "The educational foundations of our society are presently being eroded by a rising tide of mediocrity that threatens our very future as a nation and as a people. If an unfriendly foreign power had attempted to impose on America the mediocre educational performance that exists today, we might well have viewed it as an act of war."

Then, just a week later, the National Task Force on Education for Economic Growth issued a remarkably similar report. Formed under the auspices of an association of state government and education officials, the task force is perhaps a more business-oriented group than the national commission, which was organized in 1981 by the Secretary of Education. Its co-chairmen are Frank Cary, former chairman of IBM Corp., and Gov. Pierre S. duPont IV of Delaware. It also includes J. Fred Bucy, president of Texas Instruments Inc., and William C. Norris, chairman of Control Data Corp.

Except for one notable exception, the thinking of the two groups runs parallel. Education in the United States is not accomplishing what the nation needs and expects, they say, and broad and basic changes are needed. For example, the national commission's report wants emphasis on what it calls the new basics—mathematics, science, computer science, English, and social studies. Also, students should spend more time in school—perhaps an additional hour a day and as many as 40 days more each year—as well as do far more homework. The panels also maintains that teachers should receive higher pay and work 11 months.

We wholeheartedly agree with the recommendations of both bodies. Not only is an informed and literate citizenry essential to the future health of democracy, but the electronics industries have a vital stake in having available future generations of young people who are well-versed in science and mathematics. If nothing else, the reports are valuable additions to the growing chorus calling for more awareness of the value of high technology to the U. S.

But the overriding question is, "Where will the money for the longer school years and financial incentives come from?" The Federal government has already demurred, and financially strapped states and municipalities simply cannot provide it. The two reports have no answers; for example, the commission offers no advice, stating instead the truism that "excellence costs, but in the long run mediocrity costs far more."

One possible avenue of financing would be to divert funds from weapon systems to education. Such an action should actually pay off in a technologically more sophisticated citizenry and a vastly increased pool of scientists able to contribute more to the common defense.

To those who would object to any defense cuts, it is worth pointing out that the upshot would be Americans able to handle the increasingly complex weapons needed for defense. But more than that, the nation would be doing a better job of preparing its citizens to live and compete in an increasingly technological age and in a world where other nations are doing a better job of educating their citizens than the U. S.

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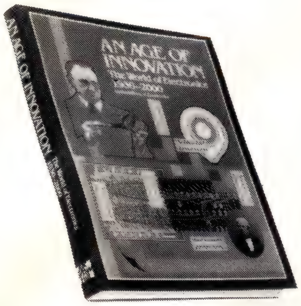

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People

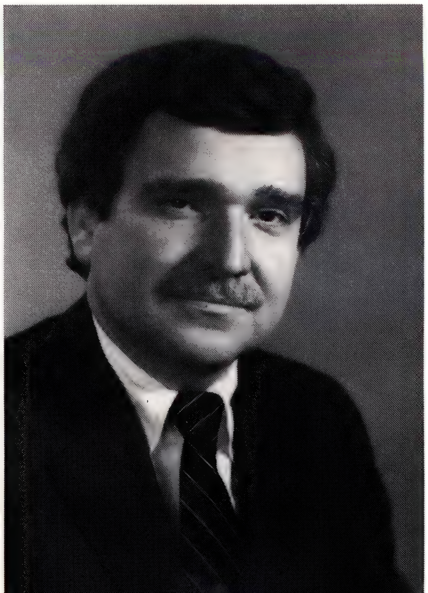
Anderson leads Ztel into next generation of PBX gear

The solemn old textile mill straddles neglected Boston & Maine Railroad tracks, once a stop on the venerable freight route. It is a massive and gloomy building; inside, the ancient elevator, a claustrophobic's nightmare, creaks slowly and indecisively between floors.

But when the doors open on the third floor, the atmosphere abruptly changes. Suddenly, it is bright and the pace quickens, for these are the Andover, Mass., headquarters of Ztel Inc., a company with ambitious plans that belie its antiquarian surroundings.

This young firm is about to double its workforce to 200 employees by year-end as it introduces what it terms a fourth-generation private branch exchange. And presiding over it—and its upcoming move out of the rather forbidding Dickensian quarters—is newly recruited president Peter S. Anderson, until recently president of Mohawk Data Sciences' MDS Systems division.

"I've had five or six opportunities of this sort, but none appealed to me like this did," says the 40-year-old Anderson. "I think the product concept here is exactly right for the market at this time." The product is PNX, for private network exchange, which combines voice, image, and data communications through a token-ring architecture [*Electronics*, April 21, 1983, p. 56]. It is that combination of PBX and local-network capabilities that generates Anderson's optimism about the market.



Market ready. Peter Anderson says the time is ripe for PNX voice, image, and data net.

Anderson says the breakup of AT&T and the new purchasing autonomy of the operating companies along with the absence of a PBX–local-network product offering from communications industry giants has created "a market window." Moreover, he adds that Ztel has wisely tailored its token-ring architecture to the evolving IEEE 802.5 standard. The Ztel system will be demonstrated publicly for the first time at the International Communications Association meeting in Anaheim in June. Production, says Anderson, will begin in December.

A 1964 Boston University honors graduate with an AB in economics and a former holder of a Woodrow Wilson Fellowship, Anderson is pleased to return to New England from Mohawk's headquarters in Parsippany, N. J.

Freas keeps things cool for Motorola microprocessors

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For example, without lower power dissipation, many 16- and future 32-bit microprocessors may never hold up in plastic chip-carriers, says the 58-year-old native of Nanticoke, Pa., who joined Motorola in 1971.

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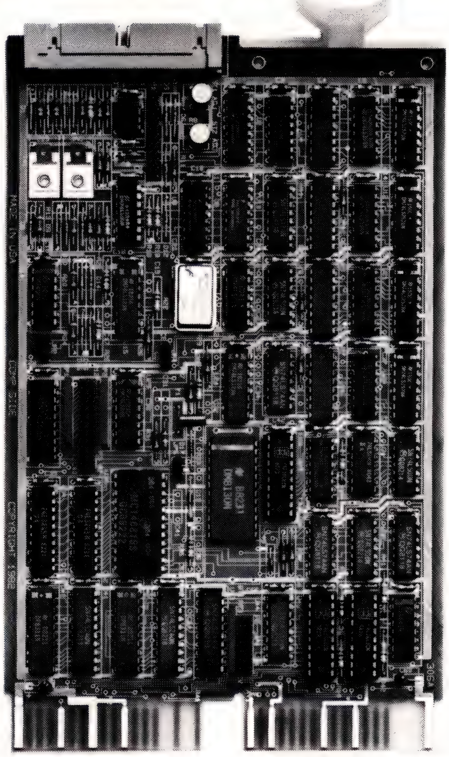

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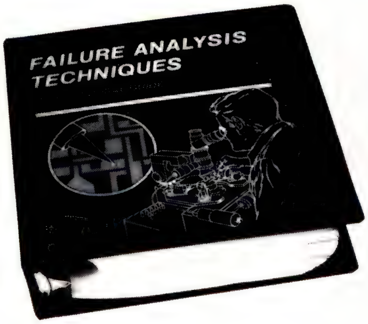

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People

Heat's off. Clark Freas says C-MOS's low power dissipation helps VLSI packages.

the problem from the inside out, states Freas, who received his BSEE from the University of Pennsylvania in 1951. For instance, he says, the firm's future 32-bit 68020 microprocessor will be made from a mixture of C-MOS and n-channel MOS in order to hold the power dissipation to 1.5 to 2 watts—about the same level as for the current 16-bit 68000 device.

Among other advantages, this will allow more flexibility in choosing packaging for the chip, Freas adds. The powerful microprocessor, which will require 100 pins, will initially be housed in what Motorola calls an R-pack, a square ceramic pin-grid array with no more than three rows of pins on a side.

Last summer, Motorola introduced the 64-pin 68000 in a plastic DIP, placing an anodized aluminum heat spreader in the package to help displace heat away from the center, where the die resides. Essentially, this cuts the heat in half, Freas explains, and shunts most of the heat to the ends of the package.

The Austin operation is also beginning to consider ways of placing the 32-bit microprocessor in low-cost plastic packages. For that reason, the division plans this month to begin studying a plastic quad pack, a square postmolded leaded chip-carrier, which will first show up in a 28-pin version to house a Motorola 8-bit microprocessor. ☐

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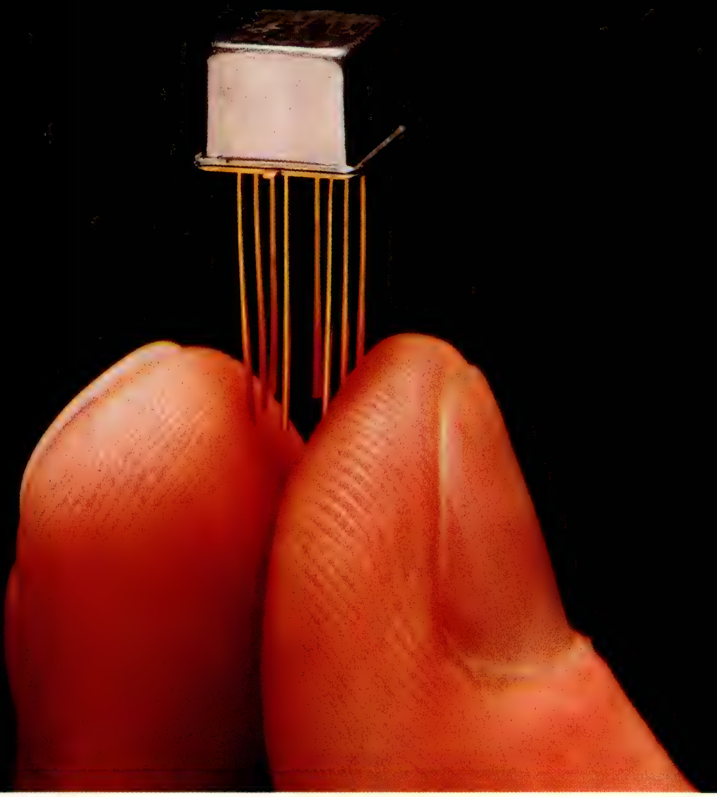

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Four scopes. Two series. One feature in common: more performance for the dollar, including a longer warranty than ever offered before.

This new generation of scopes is easier to use, more portable and more precise, to give you better measurements faster.

The 2235/2236.

Two 100 MHz additions to the Tek 2200 Series.

The 2235 features a low price made possible by radically simplified design. But it makes no compromise with Tek quality. Sensitivity, accuracy and triggering are excellent.

The new 2236 adds a microprocessor-based 100 MHz counter/timer/DMM, integrated into the vertical, horizontal and trigger systems. You get direct digital readout of Delay Time. Δ-Time accuracy to 0.001%. Plus independent floating 5000-count DMM.

The 2445/2465.

The new 2400 Series portables eclipse the 465B, the previous industry standard.

In sweep speed. Triggering. Accuracy. Number of channels. And much more.

The new 150 MHz 2445 and 300 MHz 2465 scopes are more sophisticated in performance, yet simpler in operation than any

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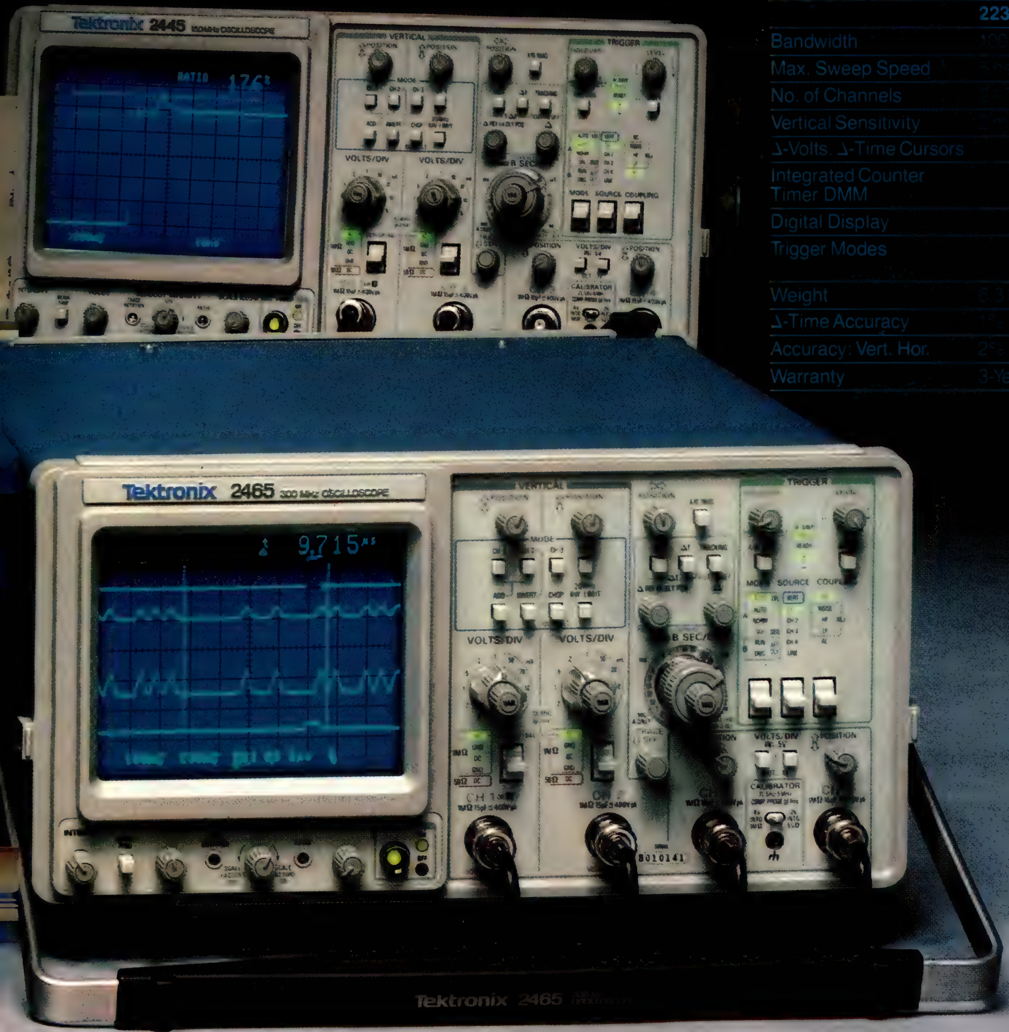
THE ANSWER BY
ANY MEASURE

Announcing four great scopes all at once!



	2235	2236	2445	2465
Bandwidth	100 MHz	100 MHz	150 MHz	300 MHz
Max. Sweep Speed	5 ns/div	5 ns/div	1 ns/div	500 ps/div
No. of Channels	2+Trig View	2+Trig View	4	4
Vertical Sensitivity	2 mV/div	2 mV/div	2 mV/div	2 mV/div
Δ-Volts, Δ-Time Cursors			Yes	Yes
Integrated Counter Timer DMM		Yes		
Digital Display		Fluorescent	CRT Readout	
Trigger Modes	P-P Auto, Norm, TV Field, Single Sweep		Auto Level, Auto, Norm, Single Sequence	
Weight	6.3 kg/13.8 lb	7.4 kg/16.2 lb	9.8 kg/21.3 lb	9.8 kg/21.3 lb
Δ-Time Accuracy	1%	0.001%	0.5%	0.5%
Accuracy: Vert. Hor.	2% 2%	2% 2%	2% 1%	2% 1%
Warranty	3-Year including CRT		3-Year including CRT	

portable scope ever designed. With features like auto level "hands-off" triggering. Standard delayed sweep Δ-Time up to 0.5% accuracy. On-screen vertical and horizontal cursors. CRT digital readouts, including time, voltage, frequency, phase, ratios and trigger level. Plus probe propagation delay matching. Four-channel capability and rugged design!

All four new scopes feature designs so simple, yet so advanced, that their reliability is backed by the industry's first three-year warranty —including the CRT.

For more information contact your local Tek Sales Engineer. Or call the Tek National Marketing Center: 1-800-426-2200, ext. 66. In Oregon, call collect (503) 627-9000, ext. 66.

We'll change your expectations of what a scope can and should be. Again.

Tektronix
COMMITTED TO EXCELLENCE

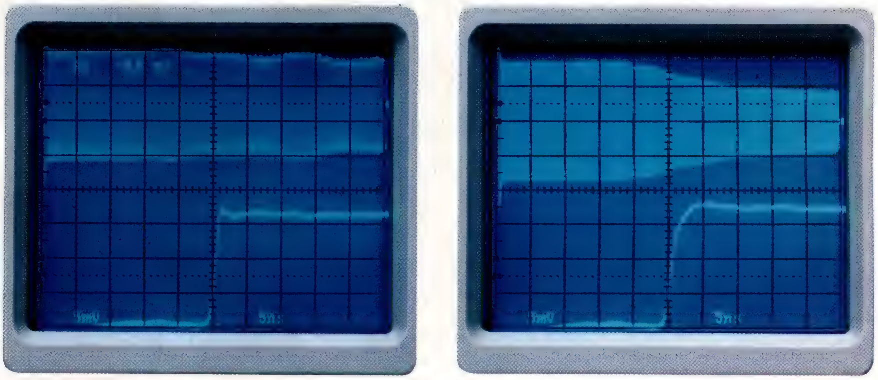
Circle 19 on reader service card

Tek challenges commodity probes to a screen test.

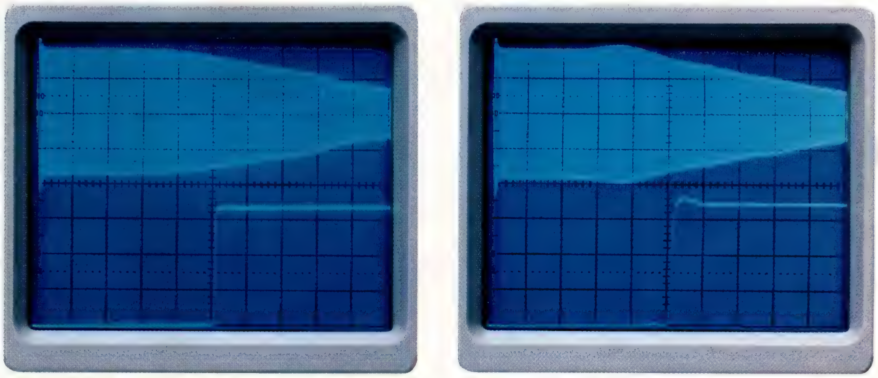
Optimum measurement results with Tek probe.

Loss attributable to a commodity probe.

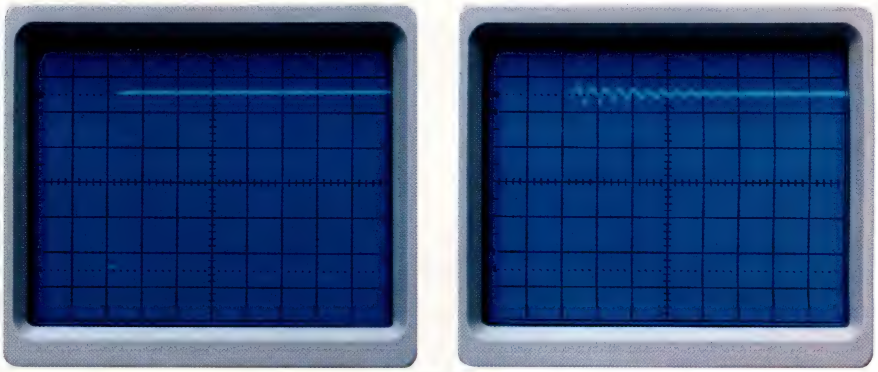
A commodity probe can act like a bandwidth limit switch. **(Left)** The Tek probe faithfully transfers a signal frequency of 300 MHz. **(Right)** But the commodity probe limits the bandwidth of the same 300 MHz scope to 200 MHz.



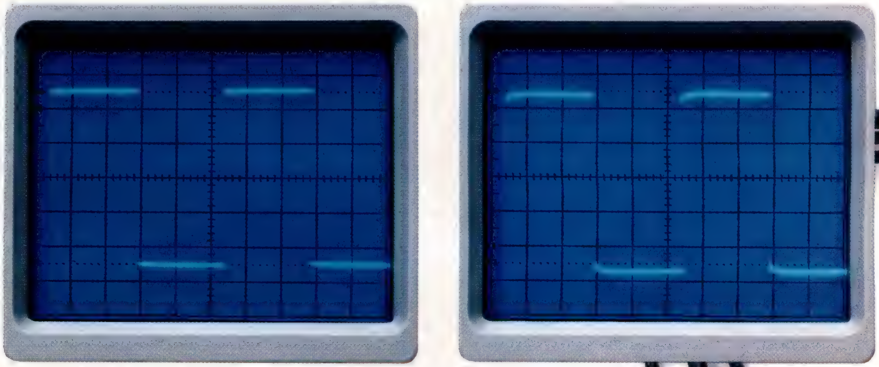
(Left) Tek probes are matched to the system throughout its frequency range for a display that exhibits a clean 100 MHz waveform. **(Right)** Many commodity probes are peaked to attain higher frequency response, resulting in aberrations.



Commodity probes don't offer a multiplicity of probe tip accessories. **(Left)** By choosing the appropriate ground lead from Tektronix, ringing simply does not exist. **(Right)** The long ground lead on a commodity probe causes ringing.



Tek probes deliver superior environmental performance. **(Left)** After 5 days of exposure to high humidity (MIL-E-16400F), the Tek probe shows no signal degradation. **(Right)** The commodity probe induces a "hook" aberration.



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See for yourself: It takes the right probe to make the best measurement!

No factor is more critical to optimized system performance than proper probe selection. A probe that's not right for your application can mean a significant loss in measurement results, plus costly delays and errors.

By giving due consideration to probe characteristics that your application requires, you can derive full benefits from the instrument capabilities that you have at hand.

For over 35 years, Tektronix has been designing probes that are matched not only to our scopes, but to your own instrument and application needs. They minimize circuit loading, while extending and enhancing system performance. By valuing the special requirements of every application, we build more value into every probe.

Bandwidth/risetime, input voltage, input impedance and limiting aberrations are all among characteristics to evaluate in terms of your own application.

And while electrical considerations are of prime importance, physical parameters such as environmental performance, cable flex life and probe length can be equally crucial. Unnecessary cable length, for example, will decrease bandwidth and increase a probe's loading capacitance:

Make your selection from the world's largest and most respected probe product line. It includes voltage probes, active and passive current probes, high voltage probes, low impedance/high frequency probes and differential probes.

Tektronix doesn't just give you more probes than anyone else. We give you probes that do more.

And to facilitate your measurement application Tek provides a wide range of probe accessories including tips, adapters, connectors and tools. These aids are described in our Accessories Selection Guide.

Call the Tektronix National Marketing Center today for an Accessories Selection Guide! It covers the entire product line, with criteria you need for matching the right probe to your application.

Call the number below or contact your local Tektronix Sales Engineer.

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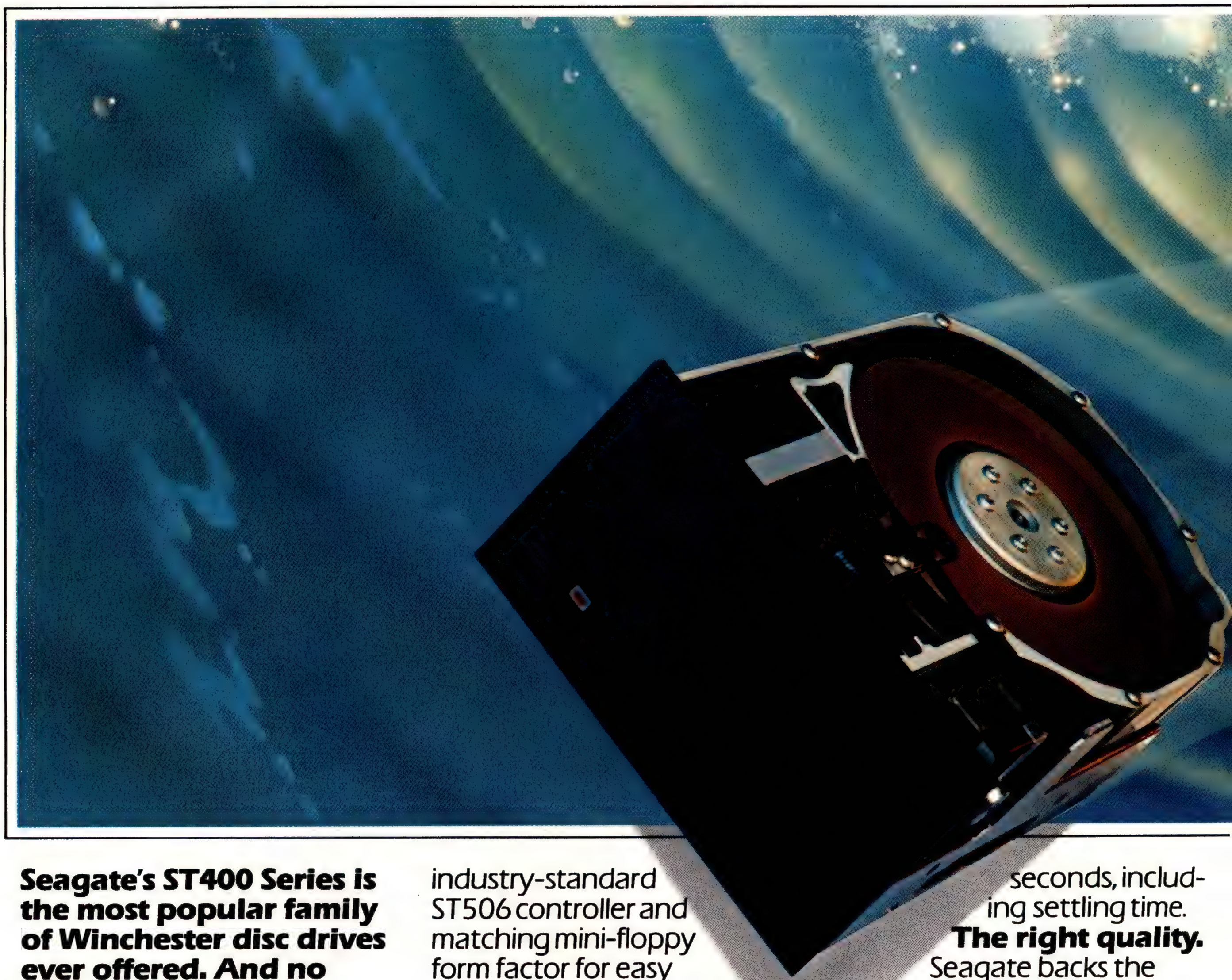

Seagate's ST400 Series is the most popular family of Winchester disc drives ever offered. And no wonder. These 5¼" Winchesters deliver more value for your money. More quality. More reliability. More performance. And all at a better price.

The ST400 Series offers the right capacities. 6.38, 12.76 or 19.14 megabytes (unformatted). All use the same industry-standard ST506 controller and matching mini-floppy form factor for easy upgrade.

The right features.

All use manganese-zinc heads, advanced stepper motor, metal band actuator, open loop head positioner, and patented air flow spindle pump. An onboard microcomputer provides buffered seek and fast step algorithm for an average seek of 85 milliseconds, including settling time.

The right quality.

Seagate backs the ST400 family with a full one year warranty, our industry-leading "105% Seagate Guarantee," and the world's biggest support team devoted entirely to 5¼" Winchesters.

Meeting special needs.

Looking for faster, more reliable removable storage? Go with our new ST706

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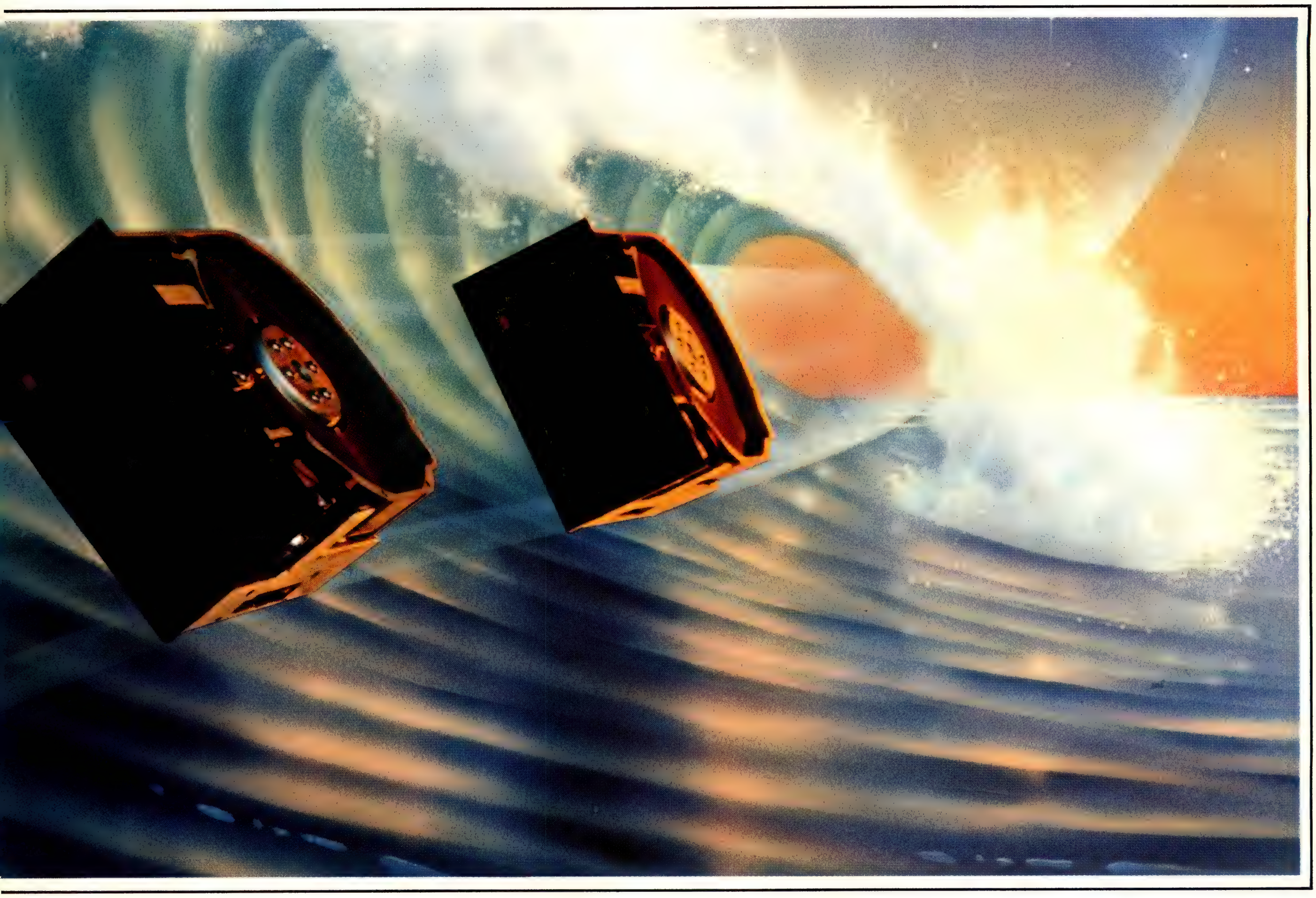

removable cartridge drive. Need a more compact drive? Pack more data in less room with our new ST206 half-high Winchester. Both new drives store 6.38 megabytes (unformatted) with reliable bit and track densities.

We have what you want in Winchester.

Selection. High volume delivery. Quality. Competitive pricing. So go with the tide. Call Seagate.

The ST400 Series

	ST406	ST412	ST419
Unformatted capacity (MB)	6.38	12.76	19.14
Formatted capacity (MB)	5	10	15
Average access time (ms)	85	85	85

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"Turning the tide in disc technology"

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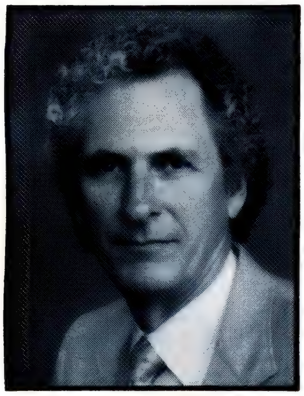
Circle 23 on reader service card

Preferred-vendor status benefits everyone

by David S. Cochran
vice president, Integrated Circuit Engineering Corp., Sunnyvale, Calif.



There is a new and controversial relationship called preferred-vendor status emerging between component suppliers and some large electronic systems manufacturers. Despite negative feelings voiced by some, particularly in regard to the effect on smaller users, I feel these emerging relationships will provide immense benefits to both sides of the supplier-purchaser equation.

A brief explanation of just how a supplier becomes a preferred vendor will help make this position clear. Of prime importance is providing products with high quality and reliability—related but separate measures of equal significance. Next is commitment to on-time delivery of the contracted quantity. Third is flexibility of supply—a preferred relationship would be of no value if the vendor could not respond to the user's needs as changes occurred in the marketplace. Last, but not to be overlooked, is cost; a competitive product position still must be maintained.

Two-way trust. All of these attributes take a number of years to develop. The foundation is built by trust in both directions—trust by the user that the vendor will continue to supply reliable products in the quantities required, trust by the vendor that the user will continue to purchase in the quantities forecast.

From such relationships spring a wealth of benefits to the component purchaser, among them a reduction in inventory. A reduced inventory can have a tremendous financial impact. A two-week savings in inventory for a billion-dollar company would save millions. Two weeks of inventory in the whole electronics business would provide enough cash for repayment of considerable debt.

A preferred-vendor relationship will result in smaller inventories because systems manufacturing companies will have little need for safety stock and none at all incoming inspection. This change will have a secondary effect in the reduced warehouse and storage space necessary to keep additional components on hand. The suspicion and distrust that has pervaded the vendor-user relationship for so long will no longer be present.

Of course, a reduction in inventory will take a large chunk—perhaps several months—out of component production that will never be produced because it would go to the now-defunct safety stock. However, this production drop may not be noticeable, depending on the upcoming economic scenario.

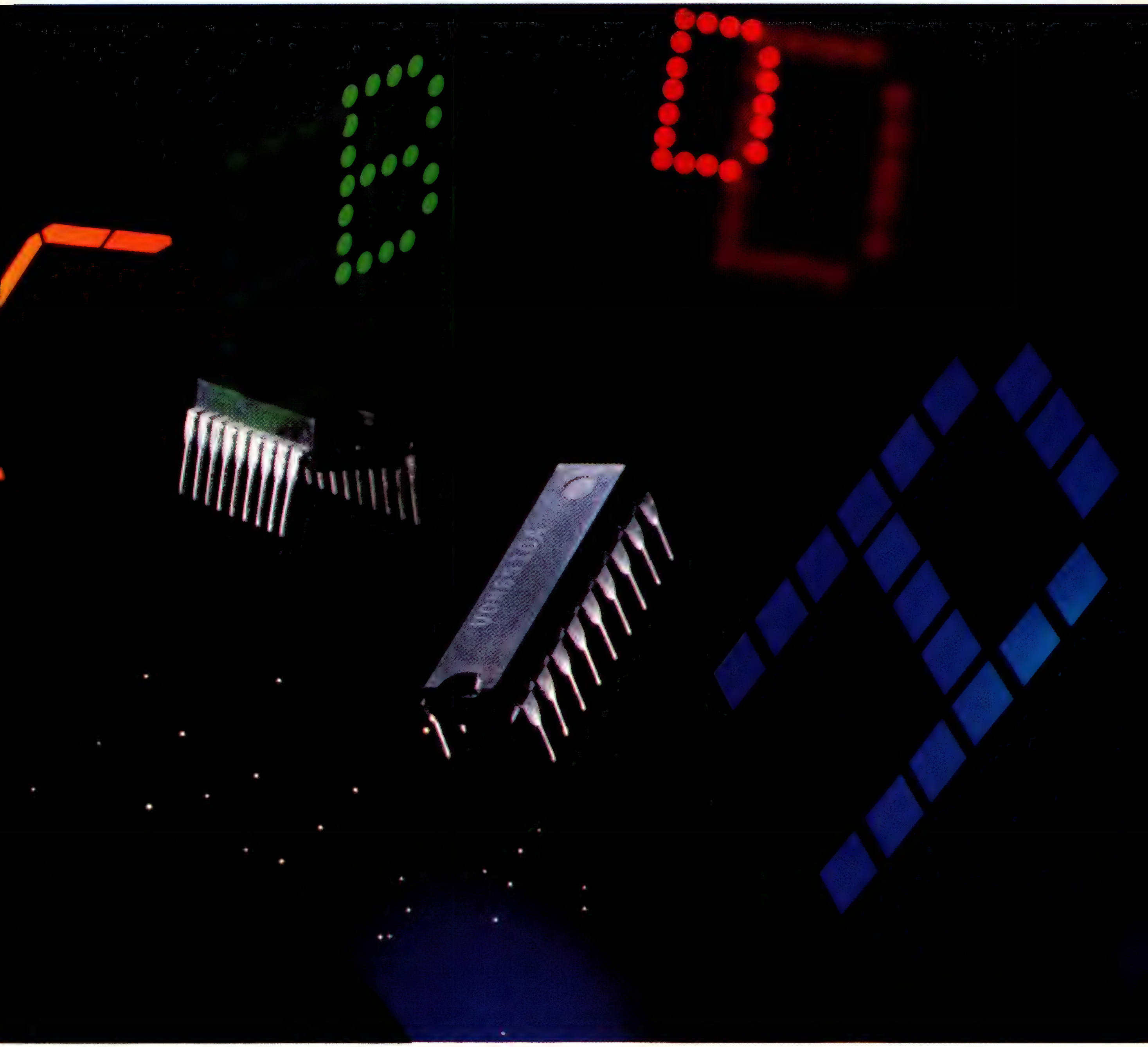
No second-sourcing. The preferred-vendor relationship will mean fewer requirements for second sources. In fact, many vendors will be a sole source. This aspect will have an economic impact in both directions. First, the purchaser will not have to exercise and evaluate two sources. He will be able to satisfy all of his needs and maintain a streamlined procurement capability with fewer sources. Second, the supplier will gain the economy of dealing with fewer purchasers and will not have to concern himself with a competitor taking over his customer.

Additionally, the preferred-vendor relationship will require less qualification effort by the vendor once he has proven himself. This improvement will eliminate multiple or ongoing evaluations and will allow a more efficient operation by both the vendor and the user. Of course, if the vendor is found in default by a quality audit, missed delivery, and so on, it will be extremely difficult for him to regain preferred status.

The argument is made that smaller purchasers, those that do not have the power to develop preferred-vendor relationships, will always get short shrift and that the preferred vendor will service only higher-priority primary users. I do not think this will happen. The long-standing fence of distrust will be cast aside. All industry parties, both large and small, will benefit from the instilled sense of commitment and dependable quality of the component supplier, joining in concert with the system maker.

Electronics *will periodically invite the expression of outside views on this page concerning issues of importance to the electronics industries.*

VISION.



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SPRAGUE ANSWERS NEEDS.

New Sprague UDN-6510A/R and UDN-6514A/R High-Voltage Source Drivers have been created in answer to the demand for bigger, brighter and easier-to-see displays. These bipolar ICs are the first low-cost 200V and 140V source drivers ever made. They will drive the anodes of gas-discharge displays or the grids and anodes of large, multiplexed dot-matrix vacuum-fluorescent panels. And they can be used in ink-jet printers. Sprague World Trade Corp., 3 Chemin De Tavernay, 1218 Geneva, Switzerland. Tel. (022) 98 40 21.
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Meetings

International Summer Consumer Electronics Show, EIA (2001 Eye St. N. W., Wash., D. C. 20006), McCormick Place, Chicago, Ill., June 5–8.

14th Power Electronics Specialists Conference, IEEE (Mark E. Snyder, Air Force Weapons Lab, NTYEI, Kirtland Air Force Base, Albuquerque, N. M. 87117), Albuquerque, June 6–9.

Conference on Optical Mass Data Storage, IEEE, SPIE (The International Society for Optical Engineering, Box 10, Bellingham, Wash. 98227), Hyatt Regency Crystal City Hotel, Arlington, Va., June 6–10.

International Conference on Consumer Electronics, IEEE (Leonard Dietch, Zenith Radio Corp., 1000 Milwaukee Ave., Glenview, Ill. 60025), Ramada Inn, Des Plaines, Ill., June 8–10.

ATE East, Morgan-Grampian Expositions Group (2 Park Ave., New York, N. Y. 10016), Hines Auditorium, Boston, June 13–16.

10th International Symposium on Computer Architecture, IEEE (Harold W. Lawson Jr., Department of Electrical Engineering, Linkoping University, 581 83 Linkoping, Sweden), Stockholm, June 13–16.

Ohmcon/83, Electronic Conventions Inc. (8110 Airport Blvd., Los Angeles, Calif. 90045), Cobo Hall, Detroit, Mich., June 14–16.

International Conference on Communications, IEEE (C. William Anderson, New England Telephone & Telegraph Co., 350 Cochituate Rd., Framingham, Mass. 01701), Boston Sheraton, Boston, Mass., June 19–22.

41st Device Research Conference, IEEE (H. Craig Casey, Department of Electrical Engineering, Duke University, Durham, N. C. 27706), University of Vermont, Burlington, Vt., June 20–22.

1983 Electronic Materials Conference, American Institute of Mechanical Engineers (420 Commonwealth Drive, Warrendale, Pa. 15086), University of Vermont, Burlington, Vt., June 22–24.

NCGA '83, National Computer Graphics Association (8401 Arlington Blvd., Fairfax, Va., 22031), McCormick Place, Chicago, June 26–30.

20th Design Automation Conference, IEEE (Paul Losleben, DARPA/IPTO, 1400 Wilson Blvd., Arlington, Va. 22209), Fontainebleau Hilton, Miami Beach, June 27–29.

Fourth International Conference on Integrated Optics and Optical-Fiber Communication, IEEE *et al.* (Melvin I. Cohen, Room 60325, Bell Laboratories, 600 Mountain Avenue, Murray Hill, N. J. 07974), Keio Plaza Intercontinental Hotel, Tokyo, Japan, June 27–30.

13th Fault-Tolerant Computing Symposium, IEEE (Michele Morganti, Telettra SpA, Via Mattel 20, 1-20064 Gorgonzola, Milan, Italy), Jolly Hotel, Milan, June 28–30.

Siggraph '83—10th Annual Conference on Computer Graphics and Interactive Techniques, Association for Computing Machinery *et al.* (ACM/Siggraph, 111 E. Wacker Dr., Chicago, Ill. 60601), Cobo Hall, Detroit, Mich., July 25–27.

Seminars

Management Skills for Engineers, Boston, June 13–15. Write Strategic Group at 266 Conant Rd., Weston, Mass. 02193, or call Prof. Harlan Platt at (617) 437-4740.

Summer courses offered by the University of California at Los Angeles include **Video-Disk Engineering,** July 6–8; **Avionics Systems Engineering,** July 11–22; **Digital Filters,** July 18–22; **Information Display Systems Engineering,** Aug. 8–12; and **Microwave Circuit Design,** Aug. 15–19. For more information on these and other courses, write to UCLA Extension, P. O. Box 24901, Los Angeles, Calif. 90024, or call (213) 825-1295.

Structured Computer-Aided Logic Design.

The Valid Concept.

Valid brings structured design to the digital logic design field, just as structured programming has brought accuracy and productivity to software development. Structured logic design is revolutionizing hardware design. We call it "No-Fault" logic design. It's the Valid Concept.

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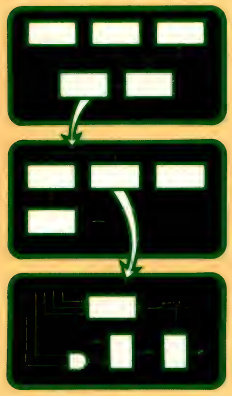
Valid's SCALDsystem™ allows you to see your design evolving interactively throughout the design process. You begin this process with a block diagram comprised of functional items that divide the design's task into major subtasks. These blocks are then defined with added detail by using easily specified lower-level blocks, and so on, down through the hierarchy. This continues until each function is described on the SCALD Graphics Design Station at the lowest level you desire.



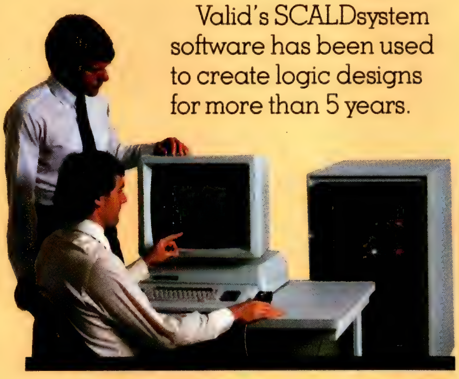
Hierarchical Design

After you enter the design through the SCALD Graphics Editor, the SCALD Compiler expands the design to form the design database. You then interactively validate the design by timing verifying and simulating the logic, making sure it performs perfectly before any physical hardware is built.

The SCALD Timing Verifier and the SCALD Simulator are the only tools you need to do this.

Once your design is validated, the SCALD Post Processor produces net lists which interface with all of the popular physical CAD layout systems.

Structured Computer-Aided Logic Design: We Invented It.



Valid's SCALDsystem software has been used to create logic designs for more than 5 years. That means our would-be competition is simply saying "me too," while our designs are field proven.

Every day, in real-world situations, we demonstrate interactive component-level logic simulation and value-independent timing verification. We invented it.

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We project that in the future all competitive logic systems from simple gate arrays through semi-custom standard cells will be designed using computer-aided engineering. With Valid's SCALDsystem the future is available now. We want you to come and see it for yourself. Remember, it was our idea in the first place, and we're years ahead of anyone else. You can be years ahead too.

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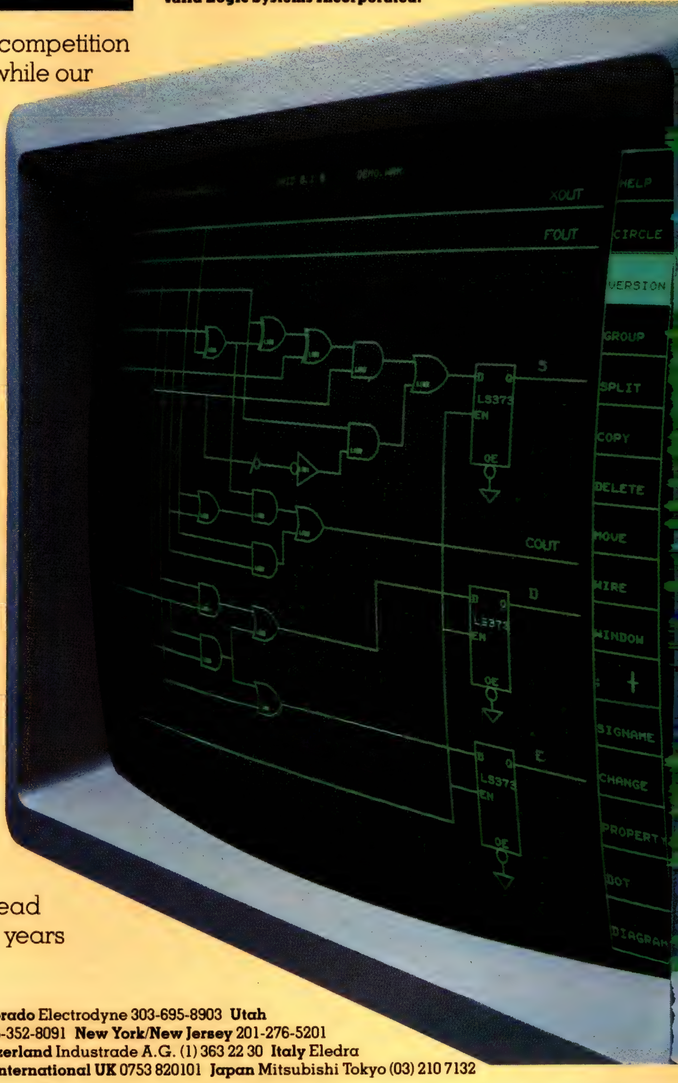

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WHAT

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Linear Vice President of Engineering. 1976 ELECTRONICS Magazine "Man of the Year." Father of the adjustable voltage regulator and many other linear standards.

CARL NELSON

Creator of the industry standard sample and hold amplifier, the first high current regulator, holder of numerous patents and is Linear's Bipolar Design Engineering Manager.

TOM REDFERN

The MOS A/D and D/A expert responsible for a lengthy list of products that have become industry pacesetters in providing interfacing of A/D's to microprocessors.

BOB WIDLAR

He started it all. Father of the first monolithic op amp, the first comparator, the first 3-terminal voltage regulator, and many other firsts.

HAVE THESE LINEAR DESIGN GURUS BEEN UP TO?

GEORGE ERDI

Well known as an elegant precision amplifier designer and responsible for introducing the industry's first monolithic D/A converter, the first precision monolithic op amp, the lowest noise op amp, and precision references, just to name a few.

PLENTY.

These five designers used to have only one thing in common. They were responsible for the design of the industry standard linear IC's that are the underpinnings of the growing $2 billion linear market. Now, they have something else in common. A company named **Linear Technology.**

In the linear world, a small band of pioneering linear designers have made most of the significant contributions to the industry. And now they've joined forces as a group to be reckoned with.

Linear Technology's truly elite team of linear designers will be soon introducing the next generation of design concepts and circuit technology.

We were created in late 1981. Now, after a period of diligent preparation, we're ready to announce the next generation of linear circuits in the areas of precision, high speed, low power, and more. And we have an extremely modern fabrication facility, the process engineers, and the processes to support our designers' concepts.

Linear Technology. Put that name in the back of your memory bank. And watch this space in the near future for the first in a series of new product announcements.

Linear. Our name may not be familiar. But the faces and reputations of our design team certainly are.

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If you just bought an LTX or

Teradyne analog test system, hide this ad from your boss.

The Fairchild Series 80 was designed from the inside out to be faster, quieter, more accurate, more efficient and more expandable than any other analog or mixed-signal tester available.

Designed for the future.

The Series 80's state-of-the-art *architecture* is unique to the industry. We were the first to apply digital signal processing to analog test solutions.

Also, we've increased efficiency for the applications engineer by coupling the bus-oriented design with a unique mainframe resource module. This makes the full power of all system instrumentation easily available, and eliminates the need for extensive fixturing at the DUT.

Finally, the Series 80 incorporates the newest-generation minicomputer products in its tester controller. The CPU speed is higher, the memory expandability is greater—up to 2MB—and the software is compatible with a wide range of CPUs, both 16-bit and 32-bit.

Ready when you are.

Another important Series 80 feature that sets it apart from all others is its true *expandability.* You start with the basic 16-channel configuration. Then, add all the capability you need—when you need it—in 16-channel increments all the way up to a whopping 256 channels! And if you have an application which requires a V/I per pin, we have it—all the way up to 120 pins!

Fast and accurate testing.

The *accuracy* of the Series 80 is the best available: .005% voltage measurement, .05% current measurement and .05% current forcing. *System noise* measured at the DUT is less than 30 μvolts. The high accuracy and low noise floor allow you to test to narrower guardbands so that you're not rejecting good parts.

The standard Series 80 has an on-board measurement system (including a nanoammeter) on each V/I source for *throughput* two to ten times faster than LTX or Teradyne.

The bottom line.

To help solve your total testing needs, the Series 80 offers a number of options, including a new low-cost Digital Resource Option. And—as part of our long-term commitment to remain your best resource for analog test solutions—we will be introducing new Series 80 system options at the rate of one per month throughout the rest of 1983.

When you add it all up, there's not an actually-deliverable analog test system on the market that even comes close to the Series 80 from Fairchild.

Sorry, LTX.

Sorry, Teradyne.

For more about the unbeatable benefits of the Series 80, call or write: Fairchild Analog Test Systems, 1601 Technology Drive, San Jose, CA 95115. (408) 998-0123, Ext. 2464. Fairchild Camera and Instrument Corporation.

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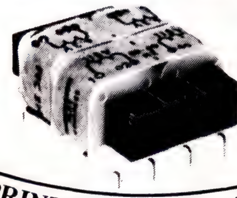
THORDARSON
FLAT COMPACT



PLUG IN PRINTED CIRCUIT TRANSFORMER

FLAT AS A PANCAKE? Yes, and because of its compact design, space is no longer a problem. The printed circuit boards of today are smaller than ever but the power needed hasn't reduced. The industry in general is the cause for better technology. The FLAT COMPACT is THORDARSON'S answer to the space restrictions of the printed circuit stacking boards in solid state control and instrumentations.

THORDARSON has the answer in 2 modest sizes. The 12 voltamp unit is 1.065 inches in height and the 6 voltamp is a mere 0.850 inches in height. The primaries being highly isolated from the secondary reduces breakdown and leakage problems. Because of this superb design, the electrostatic shield is obsolete.

The FLAT COMPACT can be used for ANY low voltage application where space is tight. Consider the FLAT COMPACT, designed by THORDARSON, for a taste of quality.

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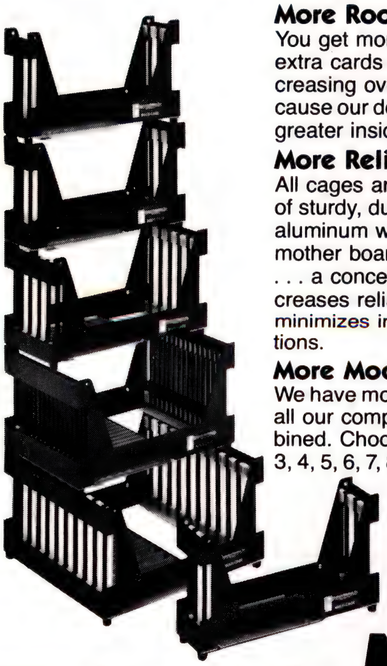

More Room
You get more room for extra cards without increasing overall size, because our design gives you greater inside dimensions.

More Reliability
All cages are constructed of sturdy, durable anodized aluminum with a single mother board backplane . . . a concept that increases reliability and minimizes interconnections.

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Circle 189 on reader service card

News update

■ Last spring, the U. S. representatives at an International Standards Organization meeting on graphics surprised some of their colleagues. They voted to accept the European GKS standard for device-independent graphics software tools and recommended that the American National Standards Institute follow suit [*Electronics*, July 28, 1982, p. 82].

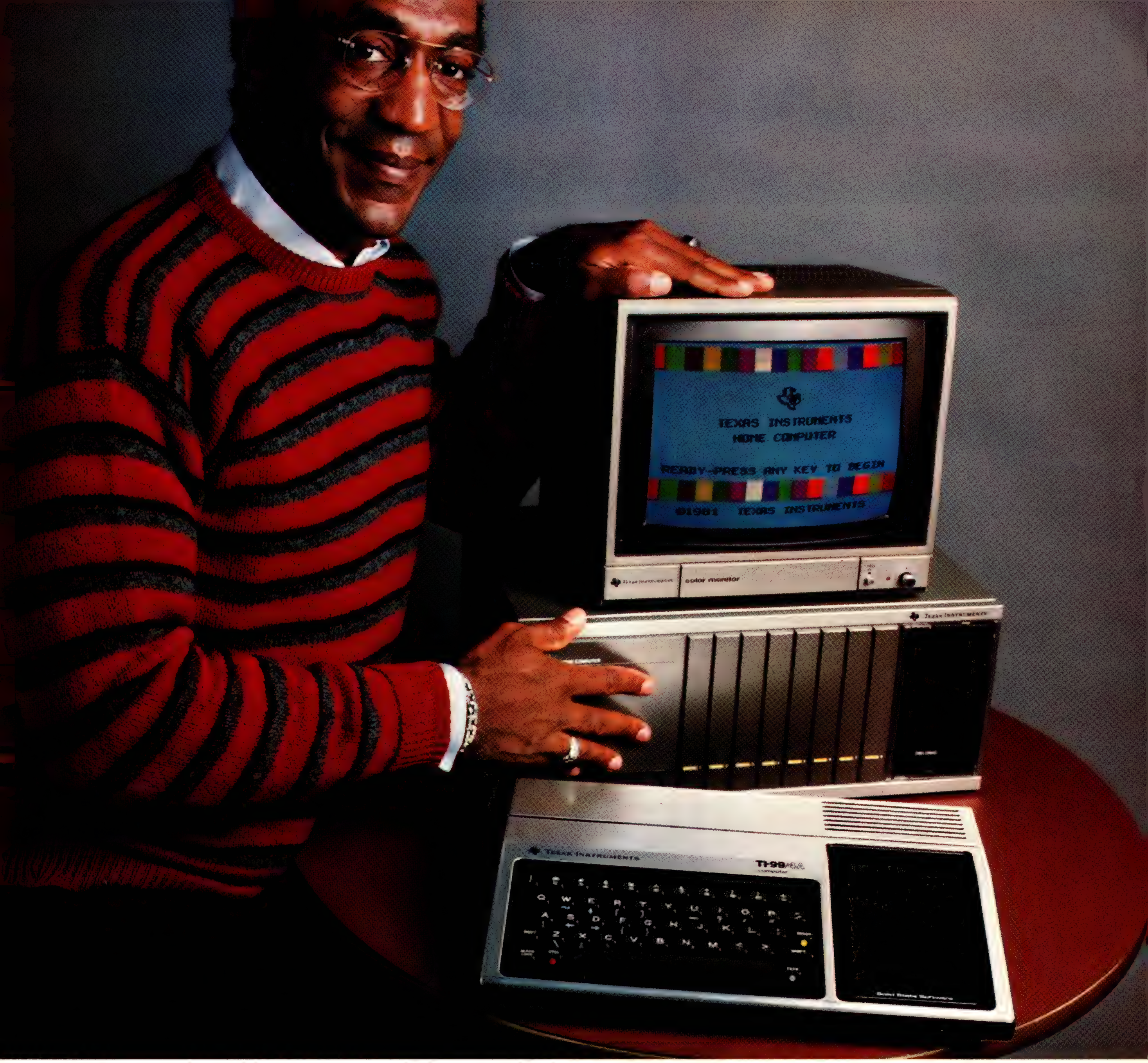
Subsequently, ANSI committee X3H3 voted overwhelmingly to seek formal approval of GKS (for graphical kernel system)—more or less abandoning the Core graphics standard developed in the U. S. and adopted by many for graphics software. However, final approval by ANSI is still at least a year away.

Core and GKS are sets of callable subroutines for use with various output devices. Though they mostly overlap, Core is held to be richer and to have more capability, GKS to be simpler and easier to implement.

Meeting now. This week, X3H3 is meeting near Portland, Ore., to discuss results of a letter ballot on GKS. The standard received 21 yes votes, 17 yes votes with accompanying comments, and only 3 nays. But this tally is deceptive: the vote is not determined by a simple majority, for a single nay raising a substantial technical issue can prevent adoption of a standard. Moreover, one committee member notes that "yes with comment" votes can pose as great a threat to acceptance as an outright negative.

In the meantime there still are no GKS-based packages on the market, though firms are working on them. James R. Warner, president of Precision Visuals Inc., Boulder, Colo., who helped write Core but voted for GKS in X3H3, says his firm has already modified its key products to comply with some GKS features. However, he adds, "It's a fallacy to think that the body of Core users is just going to dry up and blow away.

"DEC, HP, and Tektronix all have Core-based systems, and most OEMs [original-equipment manufacturers] can't tell the difference between the two." Both systems are certain to coexist in the marketplace for yet some time. **–Clifford Barney**



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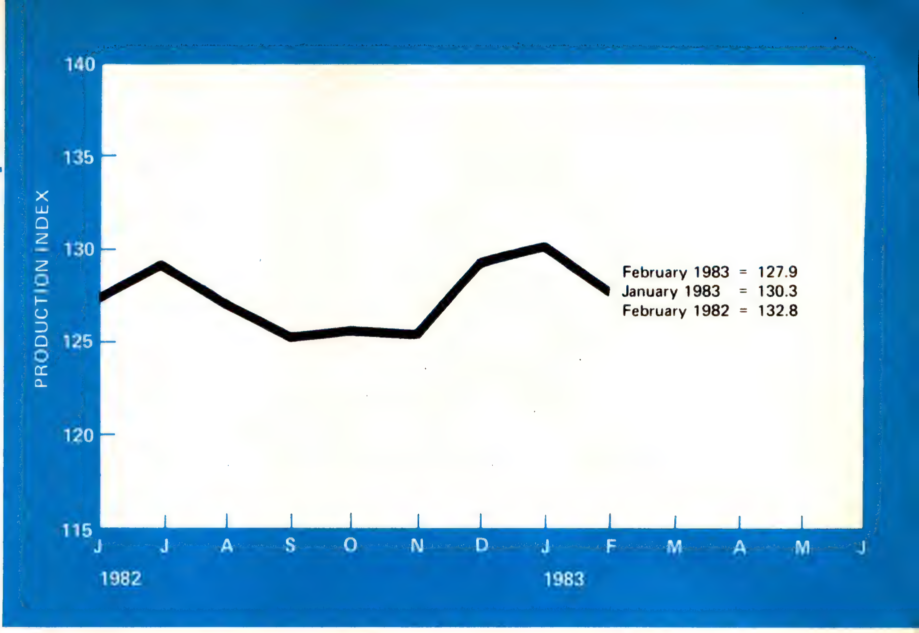
CANNON ITT
The Global Connection

Circle 34 on reader service card

Business activity

The *Electronics* production index is a seasonally adjusted measure of the level of production activity among U. S. manufacturers of office and data-processing equipment, communications and radio-television equipment, instruments, and components. As a reference point, the 1977 yearly average = 100.



U. S. INDUSTRIAL-PRODUCTION INDEX[1]

	February 1983	January 1983	February 1982
Office and data-processing equipment	242.9	250.8	256.0
Communications equipment	171.5	172.0	167.1
Radio and TV equipment	80.2	80.3	85.2
Electronic and electrical instruments	155.8 (March '83)	154.0 (Feb. '83)	163.0 (March '82)
Components	317.9	318.8	321.8

U. S. ELECTRONICS ECONOMIC INDICATORS

Production workers[2] (thousands)	February 1983	January 1983	February 1982
Office and computing machines	195.1	194.6	192.9
Communications equipment	254.9	253.9	265.5
Radio and TV receiving equipment	60.6	61.7	67.4
Components	320.6	319.4	327.1

Shipments[3] ($ billions)	February 1983	January 1983	February 1982
Communications equipment	3.859	3.810	3.742
Radio and TV receiving equipment	0.640	0.679	0.638
Electronic and electrical instruments	3.849	3.902	3.933
Components	2.411	2.408	2.341

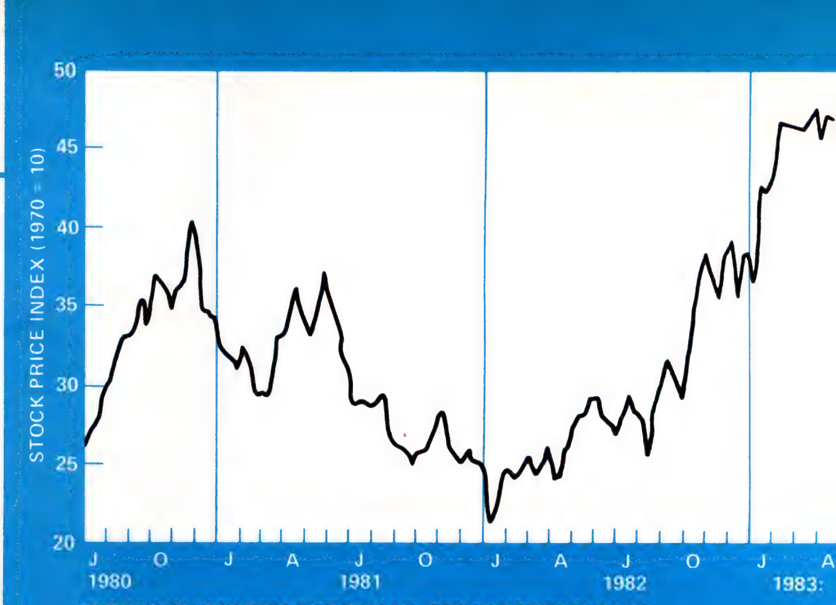
U. S. GENERAL ECONOMIC INDICATORS

	March 1983	February 1983	March 1982
Index of leading economic indicators[4]	148.3 (Feb. '83)	146.2 (Jan. '83)	135.7 (Feb. '82)
Budgeted outlays of the Federal government[5] ($ billions)	69.540	64.152	57.822
Budgeted outlays of the Department of Defense[5] ($ billions)	19.038	16.567	14.579
Operating rate of all industries[6] (% capacity)	68.1	67.4	71.8
Industrial-production index[1]	139.1	137.6	142.9
Total housing starts[3] (annual rate in thousands)	1,611	1,775	911

Sources:

[1] Federal Reserve Board (1967 = 100) [2] Bureau of Labor Statistics [3] Bureau of the Census [4] Department of Commerce (1967 = 100)
[5] Department of the Treasury [6] McGraw-Hill Publications Co., Department of Economics

Business activity



TRENDS IN SEMICONDUCTOR AND COMPONENTS STOCKS

SOURCE: STANDARD & POOR'S

The venture capital industry, depending on the viewer's perspective, is either a wonderful phenomenon or a bane to the electronics industry. Executives at established companies sometimes view the lure of venture capital as a disruptive influence, drawing capable young executives away. On the other hand, young engineers and managers, all with ideas for the proverbial better mousetrap, look upon venture capital as a way to financial prosperity. However, no one doubts that the American venture capital industry has been responsible for encouraging much U. S. technological creativity, for it has funded some of the most innovative firms in such areas as application software, computer graphics, semiconductors, robotics, and test equipment.

Venture capital investors in start-up companies can often expect a healthy return on their investment. This lure, in turn, attracts a large amount of capital. Just how much money is being drawn into venture capital can be seen from the latest data accumulated by Venture Capital Journal, a Wellesley Hills, Mass.–based publication. According to the journal, a record $1.425 billion was raised by venture capital funds in 1982, bringing the pool of available investment capital to about $7.5 billion. The $1.4 billion was committed to 54 new-venture funds and represented a 61% jump over the $867 million committed to 44 such operations funds in 1981.

Pension funds were the single largest supplier of capital in 1982, with investments totaling $474 million, or 33% of all new commitments. (In 1981, pension funds invested $200 million, or about 23% of the total.) Individuals and families were the second-largest source of new funds last year, with investments of $290 million, or 21% of the total. (In 1981, their contribution was $201 million, or 23%.) Next came insurance companies, whose $200 million accounted for 14% of the total (compared with $132 million, or 15% in 1981), followed by foreign investments of $188 million, or 13% (up from $90 million, or 10%); corporations, with $175 million, or 12% (compared with $142 million, or 17%); and endowments and foundations, with $96 million, or 7%, of total new investments (down from $102 million, or 12%).

The three major centers of the venture capital industry were California, New York, and Massachusetts, the journal points out. Venture funds in these three states together accounted for 81% of 1982 capital commitments. California-based capital commitments totaled $516.0 million, or 36.3% of the 1982 total (up from $312.0 million, or 36% in 1981). New York followed with $334.0 million, or 23.5% (compared with $115.7 million, or 13.4%, raised in 1981). Massachusetts-based funds came up with $303.9 million, or 21.3% of total commitments (up from $71.9 million, or 8.3% in 1981). **–Robert J. Kozma**

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Circle 37 on reader service card

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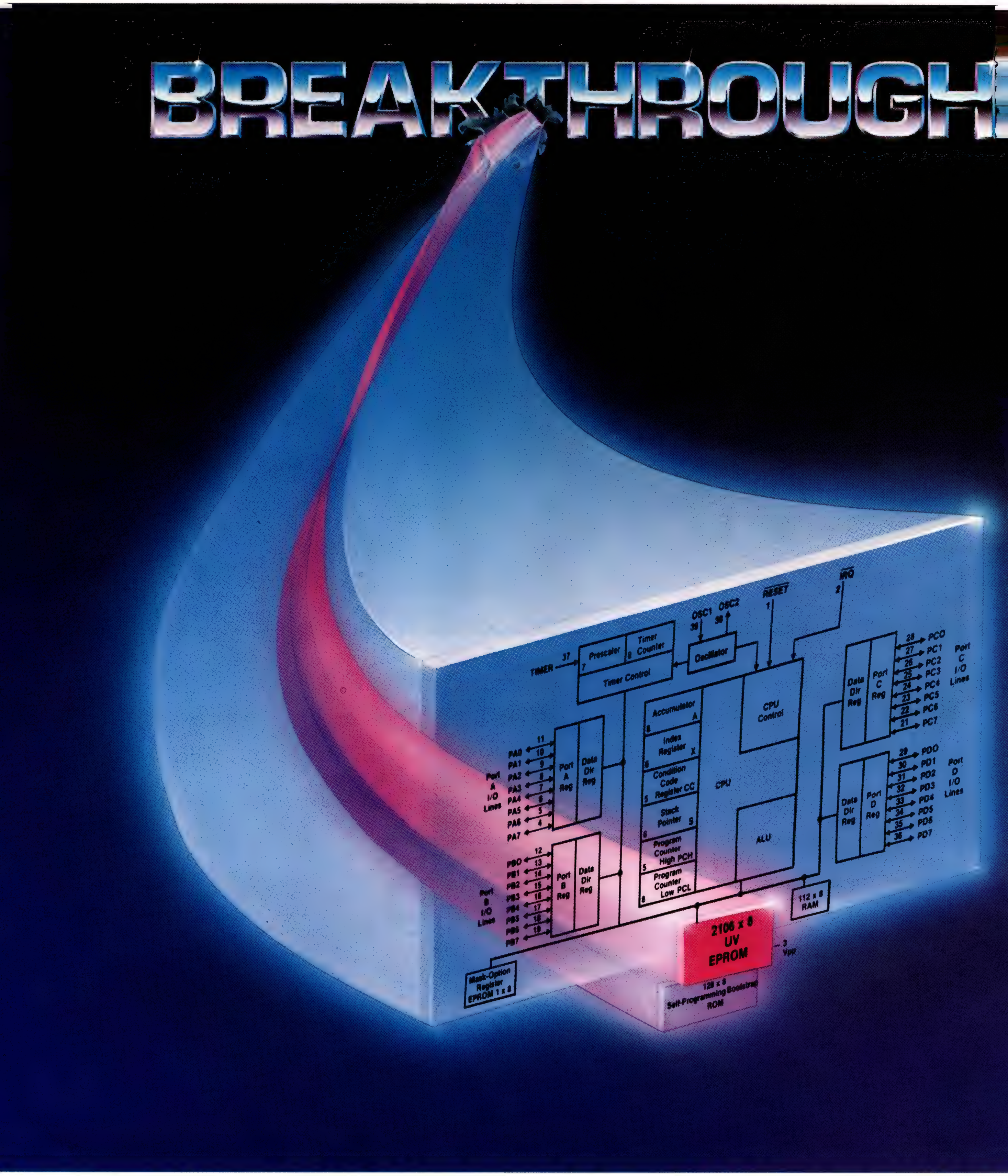


Motorola introduces the first self-programming EPROM.

And it's in volume production, oday. With a special introductory offer hat erases any doubt about price.

This powerful CMOS 8-bit microcomputer packs UV EPROM and a self-programming bootstrap in ROM—along with RAM, I/O, timer and oscillator—all on a single fully-static chip: Motorola's MC1468705G2.

The 2,096 bytes of UV-erasable EPROM will let you now run what can be a truly innovative product through ield trials and test marketing—complete prototype evaluation—and spin off interface and customer variations to an expanded market base without the delays and expense suffered from desired program changes on ordinary mask-ROM microcomputers.

Uniquely adaptive on-chip ntelligence.

Unleash your imagination with this single-chip microcomputer's unmatched flexibility in low-power environments demanding frequent program changes.

The versatile on-board, EPROM programmer routine allows the micro to actually field-program unused EPROM by as little as a byte at a time, adapting your product in real time, according to changes in data collection.

Of course, should your need for high-volume production take you to a ROM-based version of this CMOS microcomputer, the EPROM programmer is no longer necessary. In its place s a different routine that allows the microcomputer to test itself.

Unique power-saving modes.

Yes, the MC1468705G2 is low-power CMOS, with fully static operaion all the way down to DC. And yes, t thus takes but a single +3 to 5.5 V power supply.

But the power-saving magic is really n the on-chip WAIT and STOP modes.

With a WAIT mode of 0.8 mA typ and a STOP mode of 5 μA typ, the MC1468705G2's supply current is merely 3 mA at 4.5 V typ under most full-speed operating conditions.

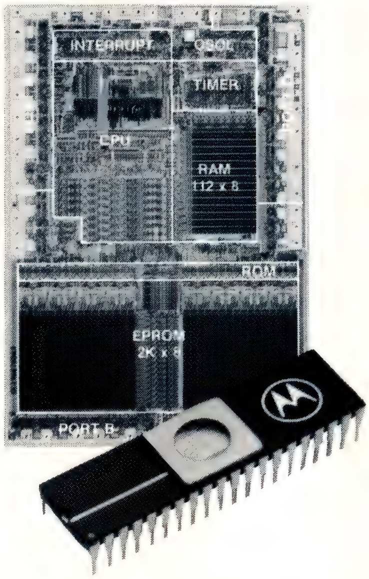
Have it both ways.

Plug in this one power miser, the MC1468705G2. Then, whether you rank out hundreds of systems or spit them out by the tens of thousands, here is no faster, cheaper, low-power way to market than with the world's irst CMOS prototyping tool.

The UV EPROM and self-programming routine let low-quantity production hit the market running as versatile field-programmable, stand-alone systems.

But, if you're going for high-volume applications, the unique user-programmable EPROM and self-programming bootstrap ROM move you quickly through field tests that can then leapfrog you straight to a pin-compatible, debugged masked ROM. With new-found confidence. And low-priced ease.

Either way, you win. With dramatically-slashed development costs and blazing-fast turnaround time.



And, when you replace existing multi-chip CMOS sets or power-hungry NMOS micros with the MC1468705G2, your customers win big also. With higher reliability and lower cost, as well as reduced size, weight and power for adaptive-intelligence applications.

To the MC1468705G2's UV EPROM and self-programming bootstrap ROM, add in 112 bytes of RAM, 4 bidirectional 8-bit I/O ports, an 8-bit timer with 7-bit prescaler, external and timer interrupts as well as software interrupt, and a master reset and power-on reset, and you've got it: the world's only user-programmable CMOS microcomputer, with unbeatable performance...straight out of the proven M6805 Family of microcomputers, with full software compatibility. And a plug-in twin of its forebear, the MC146805G2.

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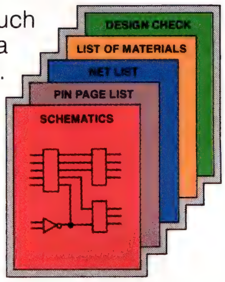

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Circle 40 on reader service card

Electronics newsletter

Seiko displays pocket color TV

Suwa Seikosha Co. of Nagano-ken, Japan—Seiko—has shown a prototype of a pocket-sized color TV set based on a liquid-crystal display of 240 by 240 picture elements that gives a picture with a 2.13-in. diagonal. The twisted-nematic display **operates in a transmissive, rather than the more typical reflective, mode;** polysilicon thin-film transistor arrays drive the device, shown at the Society for Information Display meeting. No details on availability or price were available.

Microprocessor chip makers link with AT&T for Unix . . .

American Telephone & Telegraph Co., which said in December that it would support the System V Unix operating system for Digital Equipment Corp. minicomputers, was expected to reveal agreements this week with three major microprocessor manufacturers. The announcement, slated for the National Computer Conference, was to be made by AT&T's Western Electric, along with Intel, Motorola, and National Semiconductor. Motorola will reportedly adapt its own Unix port for its 68000 microprocessor; Intel has contracted with Microsoft Inc. of Bellevue, Wash., to adapt the operating system to the Intel iAPX 286. Microsoft may also do National's 16032. **The move would mean that original-equipment manufacturers could obtain support for their systems through the chip makers,** rather than going through an intermediary that is not necessarily up to date on the latest AT&T enhancement.

. . . so software firms must find niches

The arrangement means that software houses that market Bell Laboratories' Unix or Unix-like systems will be able to maintain a market niche only by adding value to the basic operating system. However, its links to Intel and National should place Microsoft squarely in the Unix middle of marketplace. Meanwhile, the chip licensees are still waiting for tapes of System V source code; **Intel does not expect to have its System V chip ready until the first quarter of next year, and in the meantime, it has already adapted Xenix,** Microsoft's enhanced version of Unix, and will have chips by July. The announcement may also herald the release of Unix-based microprocessor products by Western Electric.

Harris pushes for C-MOS PALs by 1984

Determined to get a jump on its competition, Harris Corp. of Melbourne, Fla., intends to become the first supplier of fuse-programmable complementary-MOS logic: early in 1984 it will market the first four parts of a series to be pin-compatible with the bipolar programmable-array logic devices of Monolithic Memories Inc. and others. Designated HPL67209 through HPL67212, **the parts will hold standby current consumption to 150 microamperes and consume 5 mA/MHz in operation,** compared with a maximum of 180 mA for bipolar PALs.

Hughes uses C-MOS on sapphire for VHSIC

As its first operating device in the Pentagon's Very High-Speed Integrated Circuits (VHSIC) program, Hughes Aircraft Co. has developed a 72,000-transistor chip fabricated in complementary-MOS and silicon-on-sapphire technology. Produced for the U. S. Army's Electronics Research and Development Command, the chip is a digital correlator designed to work at 80 MHz and measures 368 by 315 mils. **The Hughes device is only the second to surface publicly in the VHSIC program,** whose managers are under tight disclosure controls.

Electronics newsletter

Zenith TV chassis sports four LSI chips

In distributors' meetings this week, Zenith Radio Corp. of Glenview, Ill., was set to unveil details of its 1984 color television line. To be known as Advanced System 3, the line boasts a new chassis design that relies on **three large-scale integrated circuits that combine integrated injection logic and linear bipolar technologies on the same chip** to replace hundreds of discrete components. A fourth dedicated LSI logic device promises improved long-term color fidelity.

Robots to get standard software package

With interest in robots increasing, the recent announcement by Computer-Aided Manufacturing–International of a program to create a standard software package for them should come as no surprise. The Arlington, Texas, organization that supports research in factory automation plans a package that would encompass all aspects of programming, control, and simulation. **The project should cost $700,000 and take three years to complete.**

Brown University to buy 10,000 work stations

Brown University will soon announce the first of a series of contracts in its ambitious program to totally interconnect the Providence, R. I., campus and 20 Brown-affiliated hospitals. The cost will be $50 million to $70 million. In all, 10,000 work stations, **one for virtually every student and faculty and staff member,** will be installed within the next five years, to be linked via a video and data network. The university would not disclose the names of the vendors.

CP/M 86 to interface with Visicorp software

The developer of the CP/M operating system for microcomputers, Digital Research Inc. of Pacific Grove, Calif., has signed an agreement with Visicorp of San Jose, Calif., to support the Visicorp's VisiON operating environment, giving users a bit-mapped interface to CP/M systems. Digital Research says **the agreement will make it easier for original equipment manufacturers to develop applications packages under CP/M 86,** the company's 16-bit operating system.

Addenda

A group seeking to bolster U. S. technological leadership has been formed in Los Angeles. Called the National Commission on Industrial Innovation, it includes among its goals "a financial environment equivalent to that of foreign competitors" and an increase in research and development incentives. **The chairman of the group's board is former California Gov. Edmund G. Brown Jr.** . . . Seeq Technology Inc., started by Intel Corp. ex-employees, is itself losing people to the entrepreneurial itch. **Four former staff members will announce a spinoff venture** founded to produce microcontrollers and nonvolatile memory components: Exel Microelectronics Inc., for now of Milpitas, Calif. . . . Kenneth A. Pickar has been named **research and development manager** of the Electronics Laboratories at General Electric Co.'s R&D Center in Schenectady, N. Y. . . . Touting it as two computers in one, Xerox Corp.'s Office Products division in Dallas will begin delivering in August a new desktop work station, the 16/8 professional computer, **capable of concurrent 16- and 8-bit processing** through its 8086 and Z80A microprocessors.

If you use any other universal programmer, it'll cost you.

Why the Citel System 47 Universal Programmer? Because the cost of ownership is dramatically less than the cost of owning any other system. The cumbersome hardware-intensive design of other programmers makes their initial cost high. Then, every time you want to upgrade, you have to pay for a costly upgrade module. It's almost like having to buy a new system every time your needs change.

The Citel System 47, on the other hand, uses a sophisticated software-intensive design. This means it costs you less to start with. It means upgrading can be done for the relatively trivial cost of additional firmware. But, more than that, since all programming algorithms are contained in the mainframe, it means over 400 devices can be programmed without having to add any hardware at all!

Use the Citel System 47 to program MOS EPROM's, MOS EEPROM's, bipolar PROM's, I.F.L., Programmable Array Logic, CMOS PROM's, and single chip microprocessors. It offers you 128K bits or 256K bits of RAM to store inputs from either a master device, serial I/O or keyboard. Fourteen different I/O formats are provided for communications at selectable BAUD rates. Operation is extremely simple and the system is compact enough to permit field use.

The Citel System 47 is one of a family of programmers that also includes the economical System 37 and System 3716 Gang Programmer for EPROM and EEPROM programming. All benefit in their design from Citel's extensive experience as the quality manufacturer of software-controlled programmers. To find out all about them, call (408) 727-6562...or, mail the coupon.

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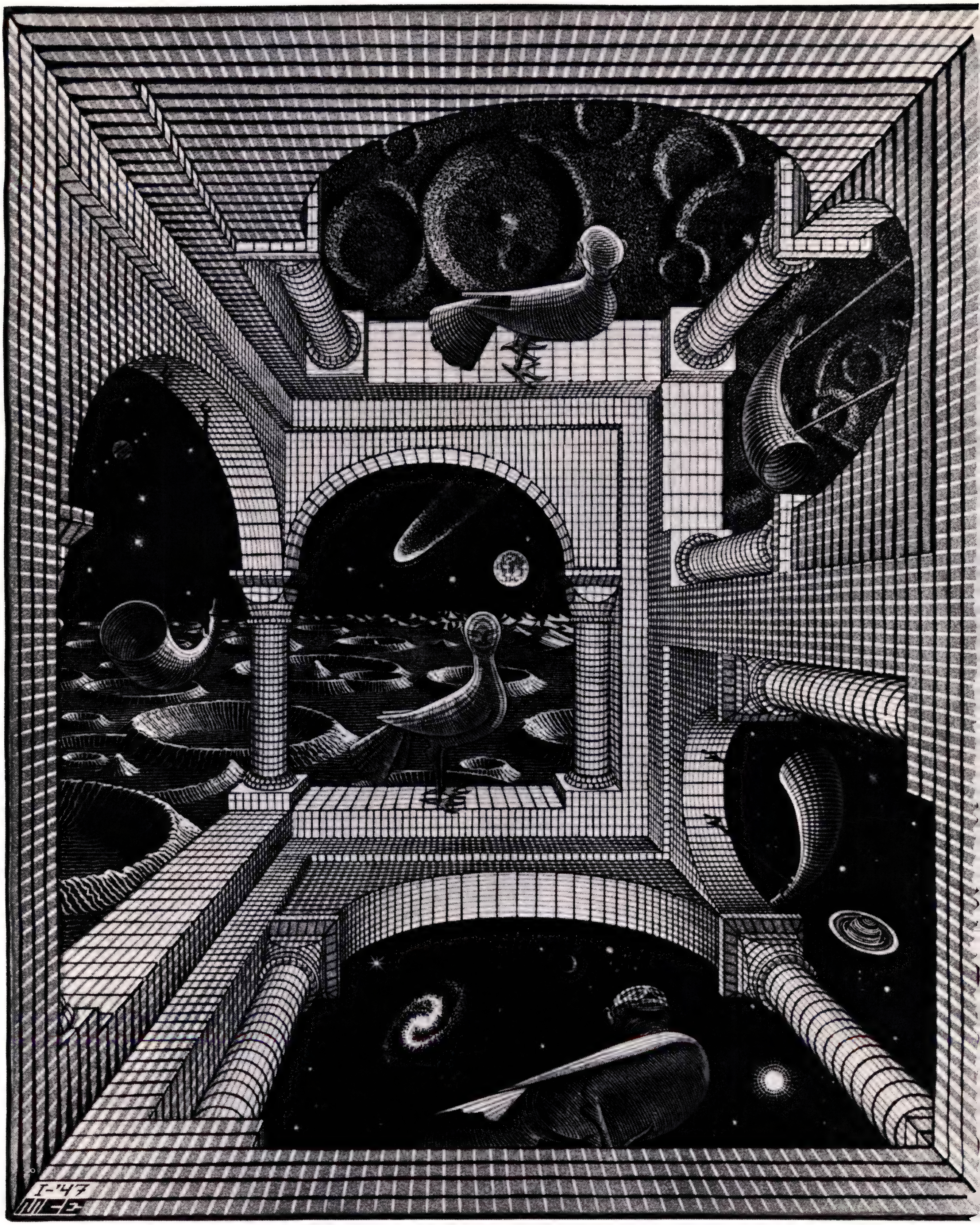

Other World, M.C. Escher, 1947.

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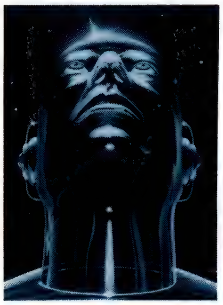

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We're taking on the future.

Portable computer accesses data base via two-way radio

by Wesley R. Iversen, Chicago bureau

Ordered for IBM servicemen, 28-oz terminal from Motorola has an alphanumeric keyboard, eliminates need for phone line

By combining its radio-design expertise with custom complementary-MOS circuitry, Motorola Inc. is about to extend the dimensions of portable computing. Its new Portable Communications Terminal is the first to incorporate a two-way radio for digital data communication. It also packs an unprecedented amount of number-crunching power for a unit its size: in a package measuring 7.75 by 4 by 1.3 inches, it carries two 8-bit microprocessors, up to 80-K bytes of random-access memory, and 160-K bytes of read-only memory.

Advantage. "To our knowledge, this is the first product that takes advantage of both rf and computer technology to provide the user with a truly portable computer that frees him from being tethered to a phone line," observes Edward F. Staiano, vice president and general manager for Motorola's Communications sector in Schaumburg, Ill. With a full alphanumeric keyboard and two-line, 54-character liquid-crystal display, the 28-ounce terminal is part of a radio data-communication system developed under contract to International Business Machines Corp. for IBM service personnel [*Electronics*, April 7, p. 56].

Deliveries to IBM are to begin in the fourth quarter. But Motorola also plans to start selling the system, the first in a new product line, to other customers in the first or second quarter of 1984, Staiano says.

The terminal's two 8-bit custom C-MOS microprocessors are patterned after Motorola's n-channel MOS 6801 family. One handles communication processing, interfacing with a custom C-MOS rf modem chip for transmitting and receiving data at 4,800 baud in the 800-megahertz band using frequency-shift–keyed modulation. The other handles data processing with a 1-megabyte addressing range. A custom C-MOS memory-mapping chip extends the normal 64-K byte range of the 6801.

The ROMs. One 256-K C-MOS ROM is dedicated to the terminal's custom multitasking operating system and several application programs, a screen editor, a file system, and calculator emulation. Four other 256-K ROMs are available for the user's application software, including a 32-K-byte plug-in cartridge. Besides its rf modem and radio, the Motorola terminal also has a built-in telephone modem for communicating outside of radio range.

In all, the terminal incorporates a half-dozen custom C-MOS devices, some of which are large-scale and some very large-scale integrated circuitry. Besides the memory and rf modem, these include a dual-ported 256-byte RAM for communication between the terminal's processors, a bus-buffer chip that facilitates fast bus operation, and a two-chip telephone modem and filter set.

These devices, in leadless chip-carriers, include 64-pad packages that take only about half the footprint and profile space of standard chip-carriers, says Ronald J. Blazek, Motorola product manager for data-communication systems. Motorola declines to detail the rf design, but points out the fit of an 800-MHz antenna entirely inside the terminal as an unusual accomplishment.

Time limit. Because a software routine limits the transmission time of any message to slightly more than one second and a maximum of 256 characters, Motorola expects to have 1,500 terminals or more on a single channel without interference. Bits in a message exceeding the 256-character limit are sent automatically as the next time slot opens up. The company expects typical messages will be only about 76 characters.

Handy item. Portable computer terminal measuring 7.75 by 4 inches has two 54-character lines of liquid-crystal display. A custom C-MOS rf modem chip sends and receives data at 4,800 baud in the 800-MHz band.

Such messages typify the use by IBM service personnel: many short computer accesses. The terminal's rechargeable nickel-cadmium battery pack should last about 10 hours with the expected seven or eight transmissions an hour, says Mary Ann Randby, Motorola program administrator for data-communication services.

Pricing is not yet set,

The portable's radio link makes the difference

"The radio link and the large amount of memory distinguish this product from other entries in what we call the hand-held computer market," observes Egil Juliussen, chairman of market research firm Future Computing Inc., Richardson, Texas. His reference is to the Portable Communications Terminal (PCT) that is part of a digital data-communications system to be sold to IBM Corp. and others by Motorola Inc., Schaumburg, Ill. Juliussen expects that Motorola may have the market to itself for a while. "It takes a fair amount of technology to do this and then to cram it all into a hand-held unit," he notes.

Already the market leader in two-way mobile and radio-paging equipment, Motorola plans a family of products in what it believes will be a significant market for two-way radio-equipped portable terminals. Some forecasts call for 20 million portable computing terminals to be sold between now and 1990, observes Mary Ann Randby, Motorola program administrator for data-communication services. "Out of those 20 million, between 5% and 15% will be radio-equipped," she predicts.

Motorola is currently working to determine the best technique for handling data communication in a cellular radio system, notes Edward F. Staiano, systems division vice president and general manager for Motorola's Communications Sector. "In a cellular system, you can spend up to 400 milliseconds during handoff [from one cell to another], in which time the channel is muted," he observes. Though this causes little problem for voice communication, it could play havoc if not accounted for in a data application. Cellular data-communication capability will probably not be offered before early 1985.

For the time being, Motorola may have its hands full meeting demand for dedicated two-way systems. IBM alone plans to link about 250 cities nationwide into its radio network. This would, for example, enable its field-service personnel to communicate with each other and with IBM mainframes for parts inventory and for equipment troubleshooting tips. Motorola also expects the PCT will find jobs in areas like financial and health services, manufacturing, freight handling, and pickup and delivery. **–Wesley R. Iversen**

though terminals should sell initially for $2,000 to $4,000 each, depending on options. The system will also include computer base stations with software for handling the rf communications in a 5-to-7.5-mile radius, as well as a central network controller that will be able to take up to 60 base stations. Each base station is expected to sell from between $15,000 to $20,000. The network controller may go for about $40,000 to $50,000. –Wesley R. Iversen

Components

Zinc oxide on MOS yields one-chip mike

By putting a thin-film piezoelectric sensor on an n-channel MOS chip, Honeywell Inc. has what it is calling "a mike on a chip" that could replace conventional piezoelectric ceramics in hearing aids and microphones. The sensor is a layer of zinc oxide deposited on a 26-micrometer-thick silicon diaphragm isotropically etched into the chip; the diaphragm is 3 millimeters in diameter.

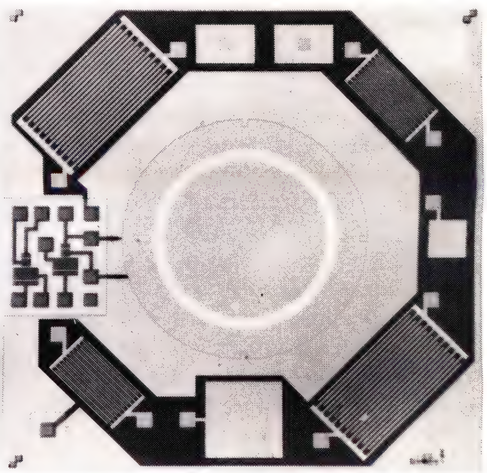
The zinc oxide layer, 2 to 5 µm thick, is laid down using a planar magnetron sputtering technique. Amplifier and other circuitry integrated into the ¼-inch-square chip complete the sensor.

Honeywell cites some important reasons why its new sensor, still a prototype, could replace conventional piezoceramic devices. It is smaller, consumes less power, and would probably be cheaper, and its solid-state nature promises more reliability. What's more, the zinc oxide–based chip offers frequency sensitivity down below 1 hertz, whereas ceramics lose sensitivity at 20 to 25 Hz, points out Michele M. Royer, principal research scientist at Honeywell's Corporate Technology Center in Bloomington, Minn.

Though researchers at the University of California, Berkeley, have fabricated piezoelectric zinc oxide accelerometers, the Honeywell device is the first reported application of the material in an acoustic sensor, says Royer. "This is a very attractive technology," she observes. "I wouldn't be surprised if our sensor is the first of many." (The Japanese have also used the material in high-frequency filters for television, Royer says.) She will describe the device at the Second International Conference on Solid-State Sensors and Actuators taking place in Delft, the Netherlands, May 31–June 3.

Vibes to volts. The Honeywell chip relies on the zinc oxide's piezoelectric properties to derive voltages from the mechanical deflection of the silicon diaphragm by incident sound. Signals from the zinc oxide go through buried contacts directly to the on-chip MOS amplifier. Encapsulating the leads in insulating silicon dioxide minimizes charge leakage and thus contributes to the chip's 0.1-Hz–frequency sensitivity.

At least one official at a U. S.-



Prototype. Honeywell's 3-mm-diameter acoustic sensor is a diaphragm overlaid with a thin film of zinc oxide that connects to an on-chip amplifier. Interdigitated devices are intended for other projects.

based piezoceramic device manufacturer, who declines to be identified, expresses skepticism over applying the new sensor in the real world. "It's feasible," says he. "Whether or not it's practical remains to be seen." But whatever its use on the outside, Honeywell research officials suggest that the chip may find volume application inside the company, though declining to say for what.

"We have a very strong interest in this technology from one of our divisions," says Ursula Kruse-Vaucienne, a business development representive at the firm's Corporate Technology Center. Assuming favorable evaluation and additional development, the chip could be ready for volume production within a couple of years, they say. –**W. R. I.**

Memory

Electronic dog tags to go on maneuvers

The U. S. Army is injecting a dose of electronic high technology into the administrative behemoth of tracking troop movements. In September, a week-long experiment run by Fort Lewis in Tacoma, Wash., will put a brigade outfitted with electronic dog tags through combat maneuvers. The troops, some 3,500 from the 9th Infantry Division, will be backed by battalion and division commands toting portable microsystems for communicating troop strength and losses.

Originally set for earlier this month, the field trial hit a last-minute software snag, according to Major Joe Burke, the liaison officer at Fort Lewis for the personnel program under the newly formed Army Development and Employment Agency. Burke is a data-processing and personnel-management specialist on assignment from the soldier support center at Fort Benjamin Harrison, Indianapolis, which is directing the Army's system-development effort [*Electronics*, March 10, p. 52].

Under the plan, each soldier will be given an electronic dog tag, called a Data Tag by its maker, Datakey Inc., Burnsville, Minn. (see "Sturdy memory device key to Army contract," above). The tag resembles a standard metal dog tag in size and weight, though at 0.090 inch it is slightly thicker. A chip embedded in the plastic, containing 2-K of electrically erasable programmable read-only memory, stores items like name, rank, serial number, and specialty.

Paperless deployment. The September trial, to be held at the Yakima Firing Center in eastern Washington, will include a full troop deployment and replacement run-through using the tags. According to Burke, the data tag of each soldier assigned will be inserted into a reader to prepare both a diskette and hard-copy passenger manifest for the Air Force as it moves troops into position. As troops arrive at the theater of operations, the tag will again be read to provide the full capabilities and status of the arriving force.

Battlefield assignments can then be made via the computer at division headquarters. Here, any shortfall in needs will be known quickly so that replacements could be delegated by computer and sent off. Tags from casualties will also be collected and, with the help of menu-driven software, a report with details to be sent to the next of kin will be generated in roughly half a minute.

Beyond the electronic tags, different levels in the division will be equipped with several types and sizes of computers. At the company level on the front line, the company clerk will use an Epson HX-20 hand-held computer to create basic reports regarding the individual soldiers and their grade, combat specialty, and status (for example, present, killed,

Sturdy memory device key to Army contract

Datakey Inc. of Burnsville, Minn., was the only company around with a portable memory device of the sort the U. S. Army sought somewhat over a year ago for its personnel identification effort, according to company president Bill Flies. As a result, it pulled down a sole-source procurement contract that called for some 3,500 of its Data Tag electronic dog tags, plus tag readers, to be used at Fort Lewis, Tacoma, Wash., in a combat field trial this fall (see accompanying story). Also, this summer, the company plans to ship about 2,000 of its new family of tags, with more memory and a microprocessor, for a peacetime application at Fort Benjamin Harrison, Indianapolis.

Privately held, five-year-old Datakey has a staff of 20 that includes five engineers. It has been a one-product firm since it sent its first product, the Data Key, to market in 1981. Since then, it has shipped 100,000 of the devices and their associated readers and control electronics to be used for controlling access to things like medical facilities and computer terminals and as a debit device in vending and copy machines.

The hardy plastic keys, each 2 inches long, contain 2-K of electrically erasable programmable read-only memory—as does the Army's Data Tag—and sell for between $4 and $7. The readers go for $20, and the interface electronics, with serial input/output and a data-management subsystem, for $15 to $75, depending on configuration. A read operation takes 375 milliseconds, writing and updating 650 ms.

The Data Tag, with similar specifications, is shaped like a standard Army dog tag. Tags and keys alike have serrated edges with gold contacts in the serrations. Readers contain gold-alloy wiper arms that sweep across the contacts during read and write operations.

The new family of keys and tags, due off the production line this month, offers EE-PROMs with up to 64-K. The devices also boast an 8-bit 8048 microprocessor from National Semiconductor Corp. for more efficient data management. Access times are faster than the simpler model: read, write, and update operations take between 100 and 500 ms, depending on the amount of data handled. Price is from $4 to $50 each in quantity. –**Marilyn A. Harris**

Electronic ID. Dog tag from Datakey, about the size of a standard metal one, contains 2-K of EE-PROM. It sits beside a reader that makes contact with the tag's serrated edges.

missing, or wounded).

This information, recorded on microcassette (future plans call for transmission by fm radio), will be passed to a larger, but still portable, microsystem at battalion headquarters that stores personnel data for the entire battalion. The clerk's report, along with a simple head count and specialty accounting done on custom-MIL-SPEC Litton Data Systems hand-held and portable computers at the battalion, will then be sent to division headquarters, which will respond with directions for troop replacements.

Traveling light. The division will have four microsystems like the battalion's, each roughly the size of a carry-on bag and weighing about 47 pounds, from Micro Source Inc., New Lebanon, Ohio. That company's M6000P/H system, built around a Z80 microprocessor, has been modified to enclose an Epson printer, half-sized hard- and floppy-disk drives, a modem, and a data-tag reader. By comparison, combat divisions currently go out into the field with two 35-foot vans full of IBM 360 equipment (though these are to be replaced with one van full of Honeywell level 6 model 47 machines).

In an actual wartime situation, the planners envision, troops will run with this setup for the first 90 to 120 days of deployment, when the front lines are still fluid. As the lines stabilize, the van with the backup computer—the "logistics tail"—would be brought to the division from command headquarters in the U. S.

Plans are also under way to modify the combat system for use in peacetime. For example, Burke says, the same tag, but with more of its 64-K memory used, would carry full personnel information and tie into the Army's master data base. In addition to basic information, the tag would store items like next of kin, previous assignments, decorations, and religious preference. Should the soldier be sent to war, however, most of that would be erased, leaving only the requirements set forth in the Geneva Convention.

Meanwhile, other military groups are exploring different means of electronic identification. This month, after a delay, the Defense Department kicks off a field trial with a "smart card," or credit-card look-alike with a microprocessor and memory, at Fort Lee, Petersburg, Va. [*Electronics*, March 10, p. 50]. Being tested is a peacetime system to control eligibility for medical and other personnel benefits. **–Marilyn A. Harris**

Business

MCC is warned of antitrust action

Some fog has settled on the rocky shoals of antitrust being negotiated by the Microelectronics & Computer Technology Corp., the research cooperative headed by Bobby R. Inman. It is in the form of a letter of protest from Joseph M. Alioto, a well-known San Francisco antitrust attorney, to each of the member companies, members of the congressional Judiciary Committee, and some California delegates.

Alioto, along with his father, the former mayor of San Francisco, recently represented Al Davis, owner of the Oakland Raiders football team, in a celebrated dispute with the National Football League over moving the franchise to Los Angeles. He contends in the letter sent at the end of January and just recently coming to light that MCC is "in clear violation of the antitrust law," and that, acting on his own, he wants to put MCC on notice that "down the road, if someone gets hurt, MCC will know that they are doing something illegal."

MCC was formed late in 1982 as a cooperative venture of, so far, 11 companies. It aims to share research and development costs in response to similar efforts sponsored in Japan by that country's Ministry of International Trade and Industry. Thus far, the Justice Department has adopted an attitude of benign neglect toward the antitrust aspects of the venture, while there appears to be growing support in Congress for exempting the company from antitrust restrictions [*Electronics*, March 24, p. 89].

Alioto's broadside was sent to the board chairmen of the companies constituting MCC as well as to the Senate and House Judiciary committees and to William Baxter, Assistant U. S. Attorney General for antitrust matters. Baxter's office has already reviewed the MCC plan and given it preliminary approval—"an amber light," as MCC chairman and president Inman calls it.

Backfire? Inman, a former Navy admiral who retired last year as deputy director of the Central Intelligence Agency, echoes the view of Peter F. McCloskey, president of the Electronic Industries Association. According to McCloskey, the Alioto letter could prove "the best thing yet" in spurring consideration and passage of modifications to antitrust statutes.

Alioto, argues McCloskey, in fact "makes the case" for the need for legislation to protect joint R&D ventures against private antitrust litigation in return for subjecting such efforts to strict government oversight and requiring them—as MCC proposes—to license resulting technology developments to any organization, foreign or domestic, for a fee. Right now there is no protection from private suits, McCloskey points out, adding that this threat seriously deters corporate participation.

The outcry against Alioto's letter, predictably, was highly charged. Control Data Corp. president Robert M. Price rebutted Alioto's antitrust "threats" on March 23 in a strong letter to Sen. Gary Hart (D., Colo.),

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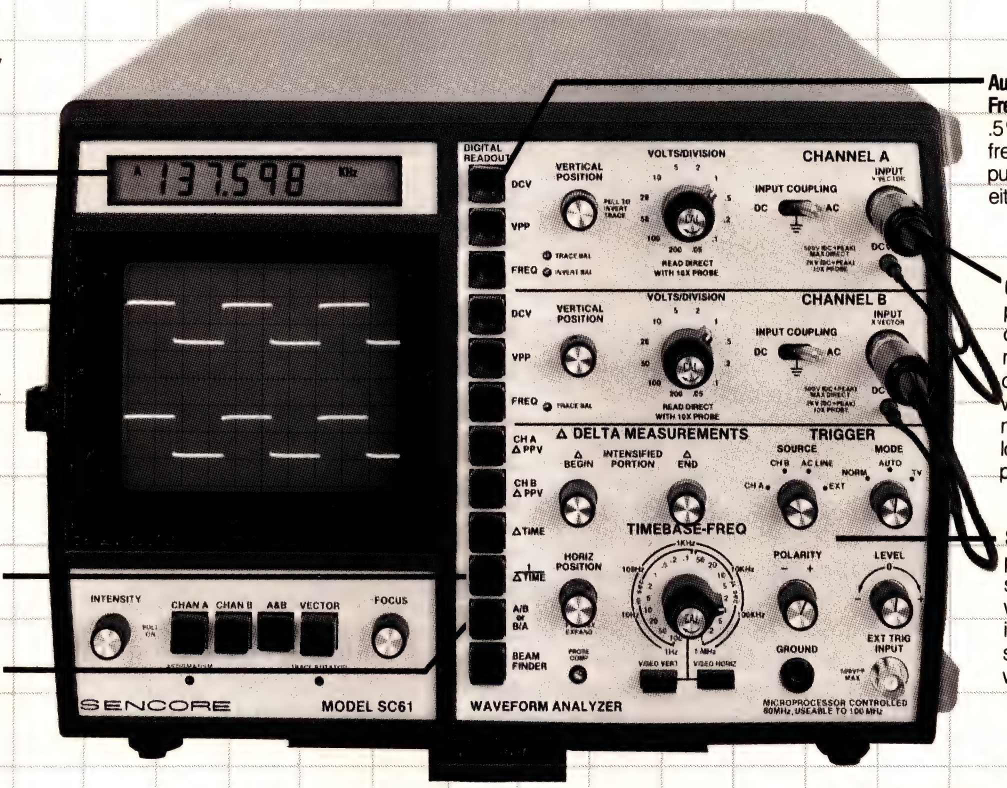

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cosponsor of one joint R&D bill with Sen. Charles McC. Mathias (R., Md.). Alioto's "unthinking and self-serving attack," wrote Price, "is a perfect example of why legislation [like Hart's S. 737] is needed."

MCC, in Price's view, is "a better alternative to the inevitable slow conglomeration of the U. S. semiconductor and computer industries that, by the turn of the century, will destroy our leadership in those industries just as surely as it has been destroyed in steel or automobiles."

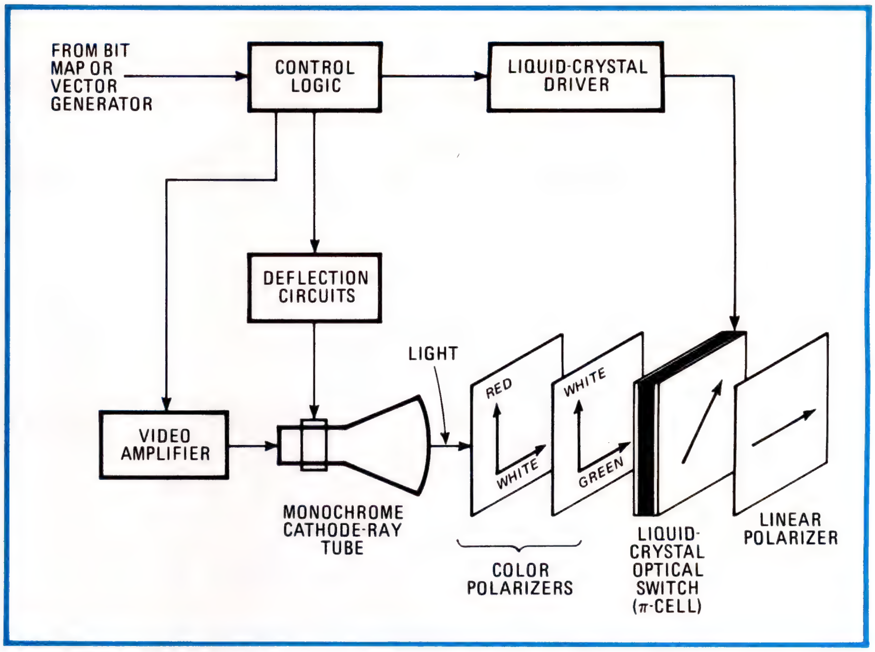
Puzzling. Alioto's motivation is somewhat of a puzzle to members of the Judiciary Committee staff, who so far have not responded to the letter. Some have speculated that Alioto is either looking for a client or that he is professing to raise a "public citizen" interest issue to get some press mileage.

But Alioto denies both charges: "I read about [MCC] in the newspaper and believe that it is a clear violation of the law. I don't believe that MCC will just do R&D—they will have a product and will eliminate competition and they will fix prices. This is completely against the American way. I'm not in this for my gain. If some small company comes to me and I do file a suit, I'll give any proceeds to a charity." **–Sam Weber**

Liquid-crystal displays

Fast LC switch handles color

A three-year research effort at Tektronix Inc. has paid off with the construction of a very fast-switching liquid-crystal device that makes it practical to build high-resolution color displays into less expensive instruments. The device, an optical switch called a π-cell, and the display, built around a monochrome cathode-ray tube, were described in two papers from the Beaverton, Ore., firm's Imaging Research laboratory at the Society for Information Display meeting in Philadelphia, May 10–12.



Display. Control logic drives a liquid-crystal switch that, by twisting light coming through two filters, lets the linear polarizer filter out emissions from a monochrome CRT. The eye integrates them into red, green, or an in-between yellow according to the area written on the screen.

Because of "the simplicity and potentially low cost" of the technique, the company is planning to employ it in small, low-cost instruments for its oscilloscope, logic-analyzer, and spectrum-analyzer lines. At the SID meeting, Tektronix showed slides of a color logic analyzer like its 1240 [*Electronics*, Feb. 24, p. 143] and a four-channel digital oscilloscope with a touch-sensitive screen that use the new display to produce red, green, and yellow. A display should be to market by early fall.

In the eye. The Tektronix system depends on the human eye to integrate color information coming through the optical switch. Light from a monochrome CRT, whose conventional phosphor has emission peaks in red and green wavelengths, first passes through red and green polarizers (see diagram). The LC switch then rotates the filter outputs so that only light of the desired color passes through a linear polarizer.

The same control logic that drives the CRT deflection circuits and video amplifier drives the color switch. By selectively writing information on the CRT—leaving out certain lines, for example—the system induces the eye to see color gradients between red and green. (Tektronix also has a prototype display that, using three color-polarizing stages and two switches, combines three primary colors into a complete spectrum.)

A similar display was described a year ago at SID by researchers from the Royal Signal and Radar Establishment in England. It uses two frequencies to switch the crystal, which makes it difficult to control the display and makes the design of display drivers more complex. Tektronix only needs a single frequency to turn the liquid crystal on or off.

The trick, says lab director George Fabel, is to get the LC material to switch fast enough. Most common liquid crystals that use twisted nematic materials switch at rates of 20 to 100 milliseconds. Tektronix required rates of 1 to 3 ms, Fabel says. The cell employs the less common tunable birefringent LC material and is built with a proprietary technique.

As described by Tektronix researcher Philip Bos in Philadelphia, the cell switches fast by overcoming a phenomenon called optical bounce. Normally, in a liquid crystal, the light-directing molecules fight being realigned by the applied electric field until the field finally forces them to line up. Tektronix changed the so-called alignment layer between the glass plates and the LC cell so that intermolecular forces aid, rather than oppose, the desired alignment.

Since the CRT in the system has no shadow mask or special patterning, the display has the high resolution of

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monochrome displays. Tektronix showed 250- and 500-line displays using 6.5-inch-diagonal tubes.

One disadvantage of such a system, Fabel points out, is that because it is field-sequential, the deflection circuits must operate at twice or three times (in a full-color version) the normal 60-hertz rate. Also, brightness is reduced to, at most, 25% of the brightness of a normal rastered CRT. But Tektronix says "it is mostly compensated for by the very high contrast of the system in high ambient light." –**Clifford Barney**

News briefs

Touch-sensitive menu replaces keyboard in executive work station

For executives with a strong aversion to keyboards, a prototype of a work station without one is being shown this week at the National Computer Conference in Anaheim, Calif., by Santa Barbara Development Laboratories Inc., Santa Barbara, Calif. Information-processing, communication, and office-automation features are all accessed through a symbolic menu presented on a touch-activated, high-resolution color cathode-ray tube. The system is geared to retrieve information from a corporate data base that is entered by others on a separate console that has a keyboard, according to engineering vice president Michael Cheiky.

The machine, whose operating system is compatible with CP/M 86, holds about 5,000 typed pages, a 500-entry telephone directory, and a two-year calendar. Voice store-and-forward, word-processing, computer, spreadsheet, and networking functions are controlled through the on-screen "buttons," as is a teleconferencing option that relies on a pair of closed-circuit TV cameras.

The computer itself is high-performance, executing 3.4 million instructions per second under control of an 16-bit 8086 processor. It has 1.25 megabytes of random-access memory; a dedicated 8-bit 8085 unit directs the voice function, and bit-slice logic controls about 80 megabytes of hard-disk storage. Price of a typical system, including an executive and a data-entry station, will be upwards of $25,000, competitive with top-of-the-line business computers, says Cheiky, who hopes to attract venture capital for production later this year.

Electron-beam lithography machines on hold

Citing sluggish demand, GCA Corp. is delaying and downplaying the debut of its long-awaited electron-beam lithography gear. Though the Bedford, Mass., equipment maker says it could ship electron-beam units sometime next year, "there just doesn't seem to be real interest in any quantity," according to director of corporate technology Griffith L. Resor III. Resor says that GCA, like others in the industry, once thought electron-beam machines would be necessary for the fine geometries of 64- and 256-K random-access memory circuits. But GCA now feels optical technologies have gained sufficient market acceptance to put electron-beam technology on the back burner. To date, notes Resor, its most significant application has been in mask fabrication.

Legislation

Senate bill seeks to protect IC designs

In its fight against chip piracy, the U. S. semiconductor industry has now garnered the Senate's support for legislation providing copyright protection for circuit designs and masks. Early this month that body introduced the Semiconductor Chip Protection Act (S. 1201), which would give 10-year copyright protection to circuit patterns, besides requiring unwitting buyers of pirated chips to pay a license fee to the originator for continued use of the design.

Sen. Charles McC. Mathias (R., Md.), who cosponsored the bill with Sen. Gary Hart (D., Colo.), said his judiciary subcommittee on copyrights, patents, and trademarks will hold the first hearings on S. 1201 on May 19. Invited witnesses include Intel Corp.'s general counsel, Thomas Dunlap; General Electric Co.'s Christopher Layton, operations vice president at the company's Microelectronics Research Center in Research Triangle Park, N. C.; Harvard University's Arthur Miller, noted law professor; and a representative of the Electronic Industries Association of Japan.

In favor. The Semiconductor Industry Association said in Washington that it strongly favors the bill, which follows years of frustrated attempts by industry to get the protection of the patent laws extended to chip designs and masks. But the U. S. Patent Office ruled that the designs as such are not patentable, a judgment that was upheld in subsequent court appeals by industry.

Patent laws protect electronic circuitry only in hardware form, but not the carefully engineered patterns that are imprinted on chips. Existing copyright laws already offer limited protection, and S. 1201 would strengthen this. It would also protect the interests of innocent purchasers of pirated chips by letting them continue to use a design if they pay a royalty to the original innovators. Moreover, Sen. Mathias points out, such payments could not be made retroactive, that is, to include the time before an infringer who unwittingly buys a pirated design is notified of a violation.

"Chip production is a fine and costly art," Sen. Mathias noted in introducing the bill, yet "innovators are being ripped off by onshore and offshore 'chip pirates,' who, for less than $50,000, can now legally appropriate and use these chip designs as their own." After photographing a chip's circuitry, enlarging it, and then making new masks, the senator points out, "the pirate firm can flood the market with cheap products," capitalizing on years of costly development by the original designer.

Intel Corp.'s Robert Noyce, an inventor of the IC and a leader in the SIA, applauded the new bill, saying: "Failure to challenge semiconductor-

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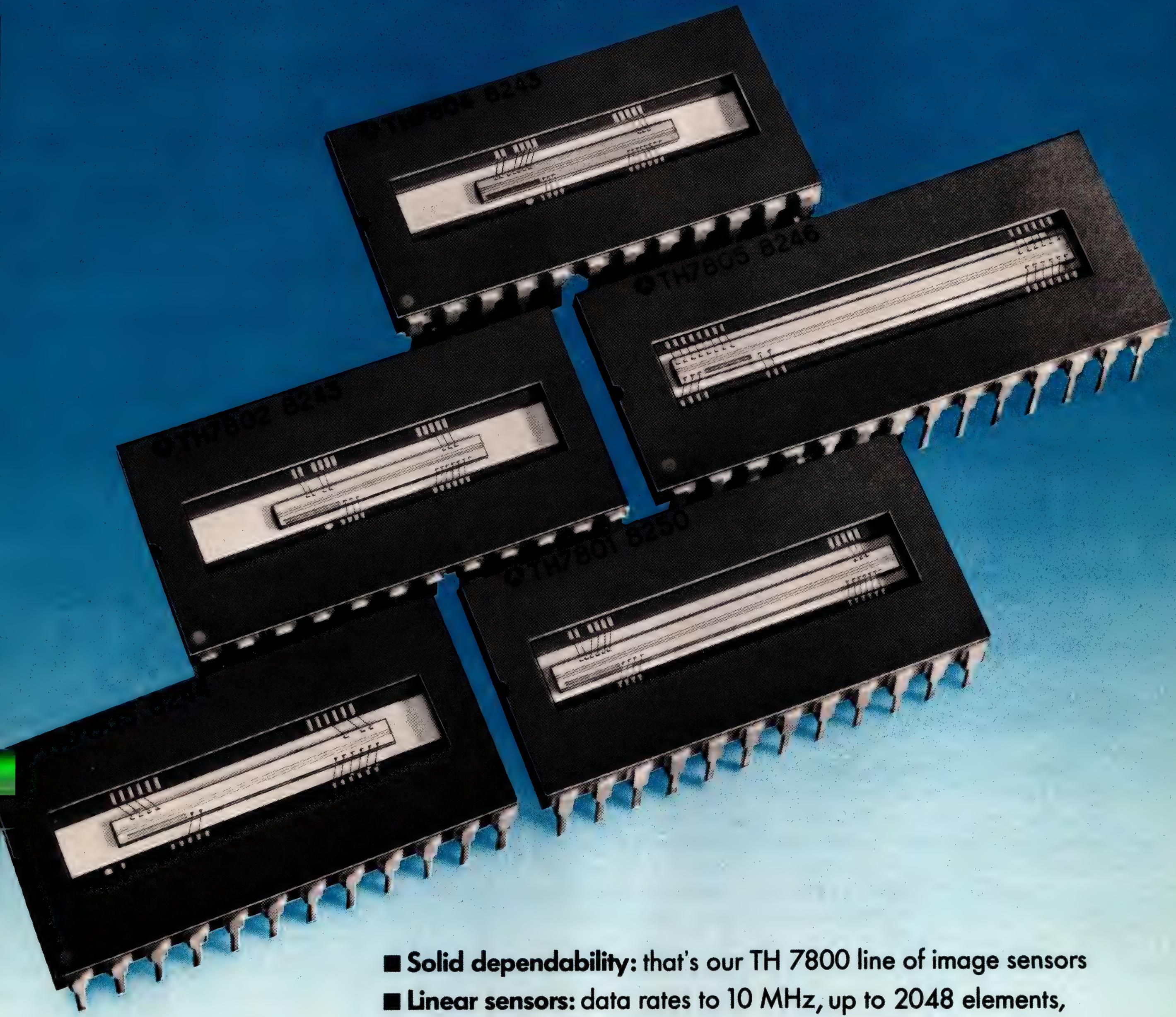

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Circle 55 on reader service card

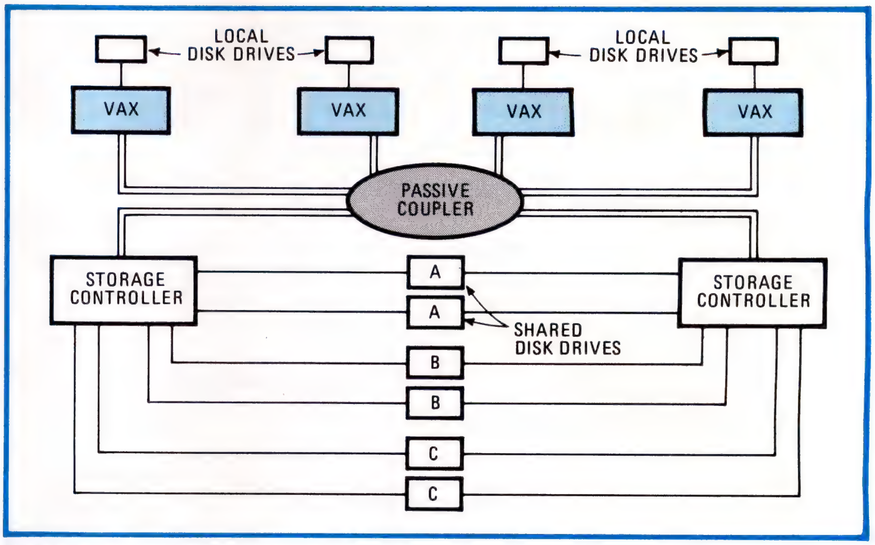
5039

chip piracy practices will have ramifications far beyond the semiconductor industry. It will reduce our international competitiveness and our national economic well-being."

Companion legislation to S. 1201 has already been introduced in the House of Representatives by California Democrats Don Edwards and Norman Y. Mineta. **–Ray Connolly**

Computers

DEC to catch up to fail-safe computers



Going fail-safe. Next year, each Digital Equipment Corp. VAX-system cluster will have redundant processors, storage controllers, and disk backup for fail-safe operation. Nodes will connect to a star coupler via 70-megabit-per-second dual-path data links, already in use.

Industry demand for fail-safe computing has fired up quickly since Tandem Computers Inc. introduced the first commercial fault-tolerant system in 1975. Though a handful of start-up competitors has since fanned the market, established vendors, for the most part, have kept out, hampered by the expensive and time-consuming task of backfitting existing machines for fail-safe operation without rendering obsolete their large software bases.

Now, an old-timer, Digital Equipment Corp., Maynard, Mass., is tackling the chore in a major effort it expects will yield big payoffs in protecting its own customer base and in competing with fail-safe vendors on their own ground. The firm recently laid the groundwork for multiprocessor, fault-tolerant configurations of its best-selling 32-bit superminicomputer family, the VAX-11 [*Electronics*, April 21, p. 41].

At stake is a market valued at $500 million last year that should climb to $4.25 billion in 1987, predicts a recent study by International Resource Development Inc., a Norwalk, Conn., market research firm. That market is dominated almost exclusively by Cupertino, Calif.–based Tandem (whose share topped 60% in 1982) and the start-up firms, which have had the luxury of building from the ground up.

The bulk of DEC's effort will go into a major overhaul of the VAX-11's VMS operating system, a project that VAX marketing manager David Chanoux says will not be completed until 1984. In the end, though, users will have the option of configuring clustered VAX-11 systems for fault-tolerant operation.

At the same time, they may enjoy the benefits of general-purpose processors for different applications using the huge base of commercially available VAX software. Also, they will not need to tailor their application programs for fault-tolerant operation, a task required with dedicated fail-safe systems like Tandem's, according to Chanoux. "By embedding such features in the operating system, we're saving users all that upfront programming work," he says.

Star. DEC this month is shipping a VMS upgrade, Version 3.3, that will support as many as 16 VAX-11/780 and -11/782 systems in a star-shaped cluster. Each processor runs its own copy of the operating system and can access all data files in the cluster, whether they are local to another processor or shared through DEC's HSC50 mass-storage subsystem. By August, VMS Version 3.4 will connect VAX-11/750 systems as well to the so-called VAXclusters.

In 1984, the firm plans to unveil a radically retooled version of VMS. Its extensions will include support for data-protection measures like redundant storage and synchronized access of files to maintain up-to-date copies throughout the cluster. Other extensions will automatically reconfigure the VAXcluster to assume the duties of a failed node. Possible too will be automatic "rolling back" of a file or even the entire contents of a data base to an earlier, known state if an error or failure occurs.

Coupled clusters. Individual computers link up by means of a passive star coupler, connected by DEC's 70 megabit-per-second dual–data-path Computer Interconnect bus (see figure, above). Maximum distance between any two nodes is 90 meters. A minimum VAXcluster of two VAX-11/750 systems will cost about $300,000; an installed VAX-11/750 or -11/780 can be expanded into a basic cluster with a package that costs just under $200,000 and includes a second processor with memory, the star coupler, and a processor interface to the interconnect bus.

With DEC's $32,500 mass-storage controllers, VAXclusters expand their power even more: a 16-processor cluster could pack more than 100 gigabytes of disk storage. Indeed, one attraction of the VAXcluster comes from the processing punch of the 32-bit VAX-11 itself, Chanoux says. Tandem machines, which also can be clustered, are 16-bit processors, and other fail-safe vendors like Stratus use processors with 32-bit data and 16-bit addressing. **–Linda Lowe**

Circle 57 on reader service card →

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COMPANY
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THAT'S WHY WE'RE THREE COMPANIES.

No company that builds a wide range of disk drives can provide the same efficiency and economy as a manufacturer that specializes in doing one thing better than anyone else.

Delays on one product affect the other lines. Inventory and labor costs are difficult to control. Research and development lag, and what was once leading edge technology becomes yesterday's news.

That's why Tandon Corporation, from its inception, has organized itself as a series of companies by product line.

There's our 5¼" Floppy Company. Our 5¼" Winchester Company. And our 8" and 3½" Floppy Company.

Each is an autonomous entity, a specialist in its own complex field with all the resources of a separate company from purchasing to engineering and quality control. Our companies can concentrate their energies on producing what they know best better than anyone else in the business. That concept is what's made each a world leader in its particular product line.

Our companies are all free to organize themselves internally to maximize their efficiency and economy and to allow them to respond rapidly to their fast-changing markets. They each do things a little differently. But all three are the most successful disk drive companies you ever heard of.

And they're all named Tandon.

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5¼″ WINCHESTER COMPANY

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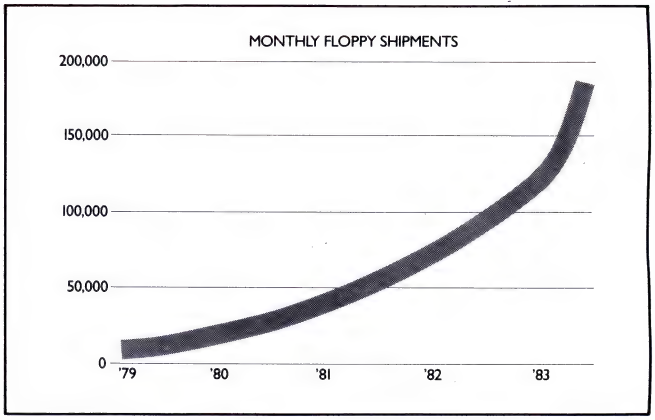
8″ AND 3½″ FLOPPY COMPANY

375 CONEJO RIDGE AVE.
THOUSAND OAKS, CALIFORNIA 91360

TO BECOME THE WORLD LEADER IN 5¼″ FLOPPIES, IT TOOK A LOT OF DRIVE.



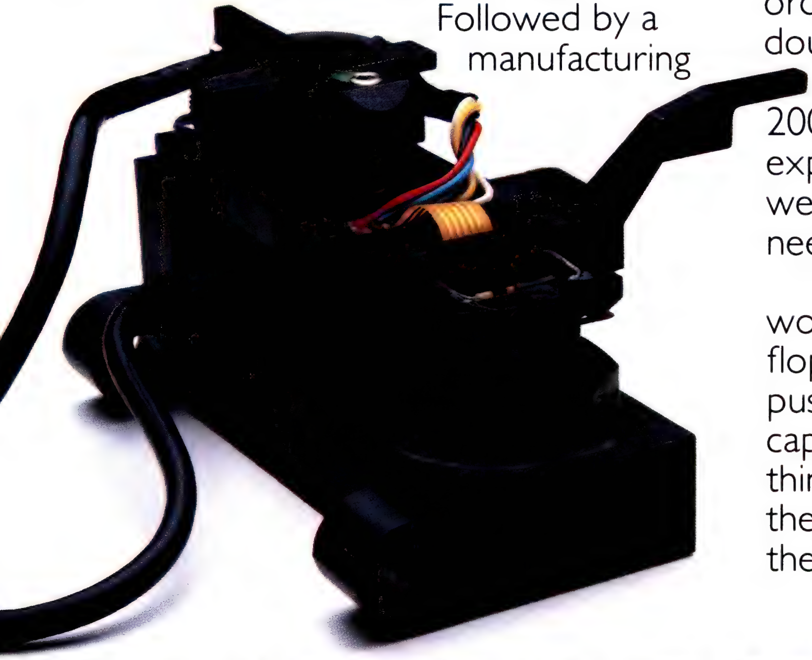
And the Tandon 5¼″ Floppy Company has plenty of drive. Both in terms of ambition and in terms of product.

Tandon's unique corporate structure lets us focus our drive on one goal: to build more of the best possible 5¼″ drives than anyone else in the world. At the lowest possible cost.

And that's just what we've done. In less time than anyone but Tandon thought possible, we've become the biggest name in 5¼″ floppies. Even bigger than such established names as… well, you know who they are. And so do they.

But all the drive in the world wouldn't have made us number one if we didn't have the product to back it up.

We do. Starting where it counts, with innovative engineering and design. Followed by a manufacturing operation that features the highest degree of vertical integration in the industry. 80% of the material cost of our drives consists of parts we manufacture ourselves. So we can keep far tighter control over quality and cost. And avoid what other companies call "unavoidable supplier-caused delays."

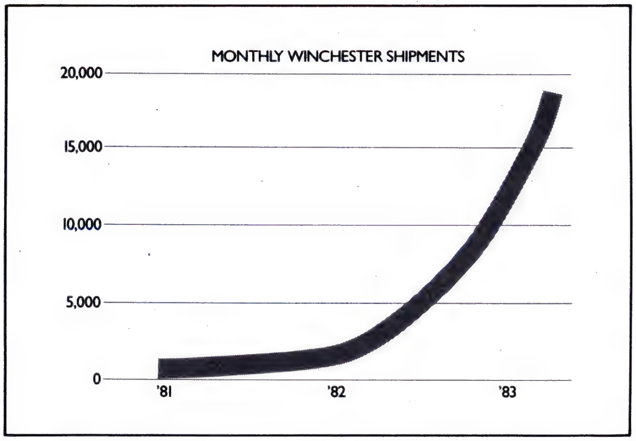


Our aim is always to maintain production capacity higher than actual orders. Last year, we more than doubled our production capacity with facilities that can easily exceed 200,000 drives a month. In 1983, we are expanding still further. To be sure that we can always deliver the drives you need, when you need them.

That's how we plan to stay the world's number one supplier of 5¼″ floppy drives. By building drives that push the limits of performance and capacity further than our competitors think possible. In greater numbers than they can produce. At lower costs than they can match.

TANDON 5¼″ FLOPPY COMPANY.

WE DON'T MEASURE WINCHESTER CAPACITY JUST IN MEGABYTES.



We measure it in terms of production capacity. Capacity for technological innovation. And capacity for building-in quality at the lowest possible cost.

We're the Tandon 5¼" Winchester Company. And we're at a disadvantage. Unlike our Tandon sister companies, we're not the world's production leader in our field. We're only number two. Though not by much. Like the Tandon 5¼" Floppy Company, we didn't start first, but we intend to finish first.

We build a wide range of drives. Open-loop and high performance closed-loop models. Right now, we have the capacity to build and ship 60,000 drives a month. That means that we have the capacity in place to be number one in 5¼" Winchesters. And we intend to be. By offering you what no other Winchester manufacturer can.

No other Winchester company makes so many of the parts that go into its drives.

No other Winchester company builds its own heads.

No other Winchester company manufactures more of its own plated media and its own PC board assemblies.

Our innovative products are backed with a 105% guarantee. Including our brand-new half-height 5¼" drives. With 6.4 and 12.8MB in half the space of traditional 5¼" Winchesters.

We're dedicated to building more drives with more capacity in less space for less cost.

Which means we're dedicated to being the world's leading producer of 5¼" Winchesters.

TANDON 5¼" WINCHESTER COMPANY.

OUR SMALLEST ACHIEVEMENT IS THE INDUSTRY'S BIGGEST SUCCESS.

The Tandon 8″ and 3½″ Floppy Company is the world's largest producer of 8″ ThinLine™ drives.

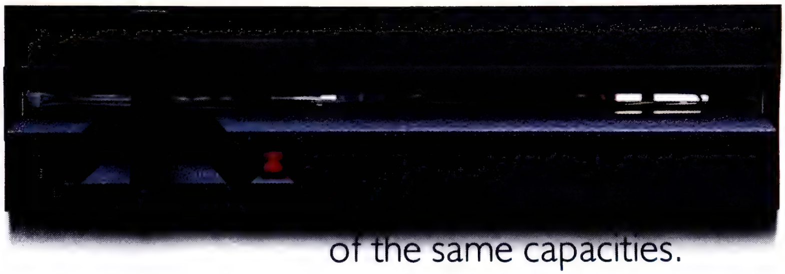
And now we're ramping up for high volume production of single and double-sided 3½″ drives.

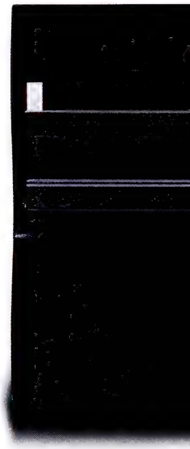
When we introduced the half-height 8″ floppy drive, we expected system designers to go wild over it.

You did. Some of you stacked two of our drives to double system storage to as much as 3.2MB without increasing system size. Others took advantage of our small achievement to reduce system size instead.

Whatever you've done with our ThinLines, we want to thank you for having the confidence in them to give us an overwhelming lead in the half-height 8″ market.

Now we're using our experience in making drives small to make them even smaller.





Our new 3½″ drives are now in production in four versions. 500K byte single-sided and 1MB double-sided Tandon interface models. And Sony interface-compatible drives of the same capacities.

We plan on becoming the world's leader in 3½″ the same way we became the world's leader in half-height 8.″ By focusing our energies on building more drives, better, at a lower cost than anyone else.

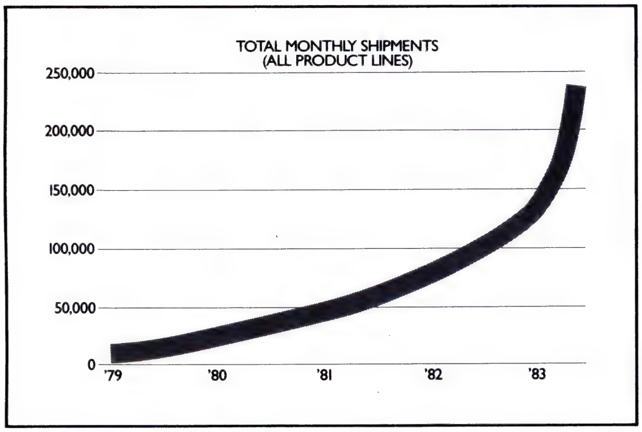
Like all Tandon companies, we start with a high degree of vertical integration. And an aggressive commitment to R&D no one can match.

We've also established ourselves in a brand-new facility with all the latest manufacturing and test equipment. So we can triple our current leading monthly production rate while ramping up to meet the burgeoning 3½″ market.

Just because we've become a success by thinking small doesn't mean our plans are modest.

TANDON 8″ AND 3½″ FLOPPY COMPANY.

WE MAKE 24 DRIVES A DAY. NO WONDER WE'RE THE WORLD'S PRODUCTION LEADER.



With 24 different drive models in production each and every day, it's not surprising we're the number one supplier of micro peripheral disk drives in the world.

We're producing upwards of 10,000 drives every business day. Over 200,000 a month. And at this rate more than 2½ million drives a year.

Here's how the Tandon Companies have become the most successful disk drive companies you ever heard of:

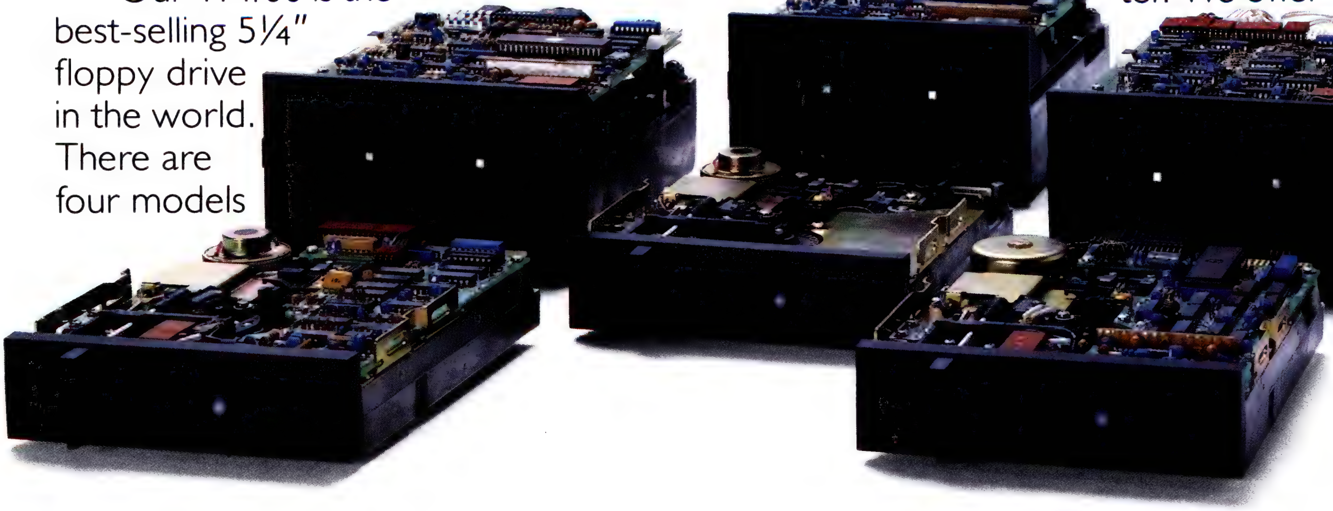
TANDON 5¼" FLOPPY COMPANY. 12 BEST SELLERS.

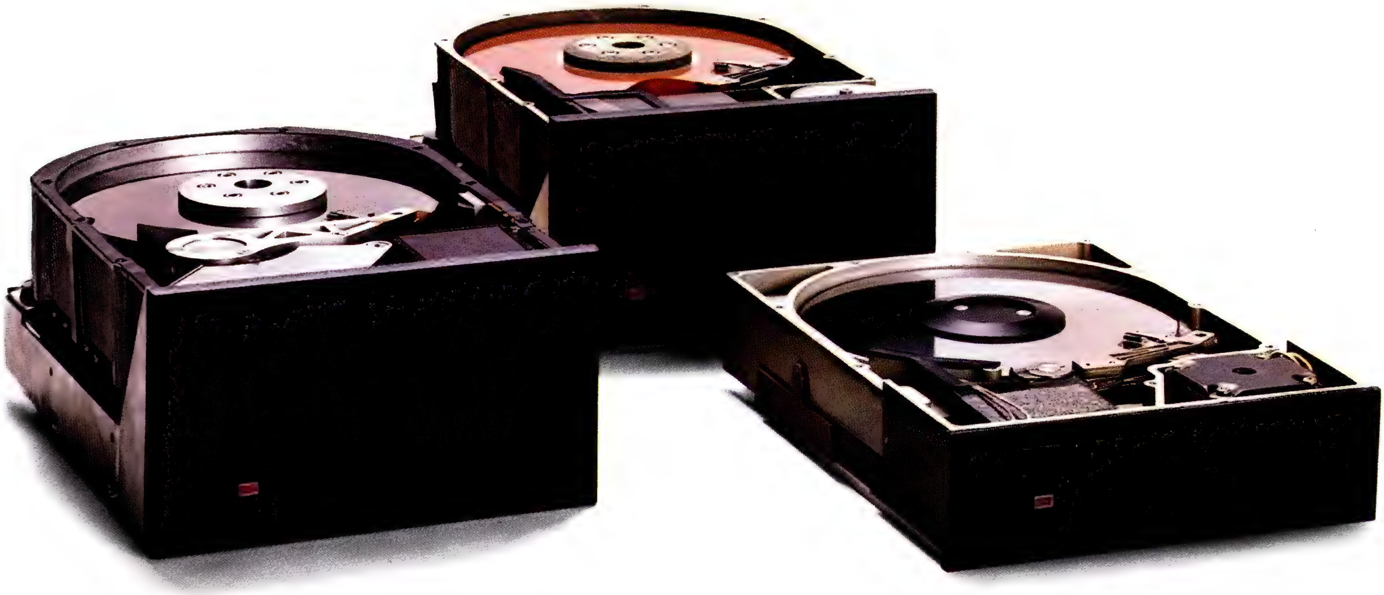
Our TM100 is the best-selling 5¼" floppy drive in the world. There are four models to choose from. 48TPI with 250KB. 48TPI with 500KB. 96TPI with 500KB. And 96TPI with 1MB. Our TM101-4 is a microprocessor-controlled model offering 96TPI with 1MB. And our TM102-2 has 96TPI with a full 2MB capacity.

Then there are our half-height 5¼" ThinLine floppies. Our ultra low cost TM50 comes in four versions. Two mechanics-only models for high-volume OEMs who want to provide their own added value and two models with fully operational electronics. Both versions come in 48TPI 250KB and 500KB capacity models. For microprocessor-controlled performance, our two model TM55 5¼" ThinLines offer 48TPI with a 500KB capacity and 96TPI with a 1MB capacity.

TANDON 5¼" WINCHESTER COMPANY. 6 DRIVES IS JUST THE BEGINNING OF OUR CAPACITY.

Our TM500 is an exceptionally cost-effective Winchester. We offer it in





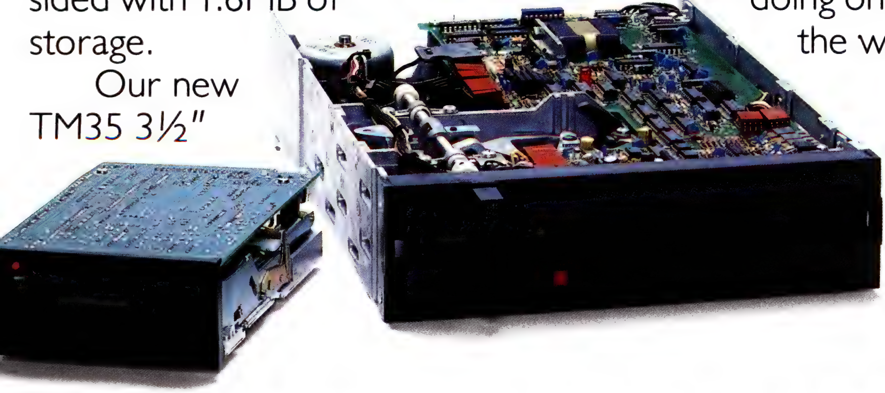
three models: 6.4MB, 12.8MB, and 19.2MB unformatted capacities. Our TM703 is a high-performance, closed-loop 5¼″ drive with a full 30MB of storage.

We're proudest of our new TM250 half-height 5¼″ Winchester. It's available now in 6.4MB and 12.8MB versions. With all the performance of a full height Winchester in half the space.

TANDON 8″ AND 3½″ FLOPPY COMPANY. 6 SMALL DRIVES. NO SMALL ACHIEVEMENT.

Our TM848, our first half-height 8″ floppy, is still the world's best seller. It comes in two models. 48TPI single-sided with 800KB capacity and 48TPI double-sided with 1.6MB of storage.

Our new TM35 3½″ drives are available in four models. Two Tandon TM100 interface-compatible versions—500KB and 1MB. And two Sony interface-compatible versions—also 500KB and 1MB capacities.



THE TANDON COMPANIES. THE DIFFERENCE IS OUR SUCCESS.

Separately, we offer products no competitor can match. Together, we're a corporation that has doubled or tripled its growth every year for the past 5 years.

Buying from the Tandon Companies offers you all the advantages of buying from a single source. *And* all the advantages of buying from a supplier who has concentrated all its resources on doing one job better than anyone else in the world.

That's the Tandon philosophy. It's given us an all-important edge on our competitors. And it's made us the most successful disk drive companies you ever heard of.

THE TANDON COMPANIES.

Tandon

THE MOST SUCCESSFUL DISK DRIVE COMPANIES YOU EVER HEARD OF.

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Washington newsletter

FCC approves a score more satcoms . . .

Twenty-two more U. S. communications satellites (including one in-orbit spare) were approved for construction and launching by 10 companies, three of which must demonstrate their financial ability by Dec. 31 or lose their authorizations. **The action by the Federal Communications Commission granted seven applications unconditionally:** American Telephone & Telegraph Co. for launching three Telstars; American Satellite Co. for two launches plus one ground spare; Hughes Communications Inc. for launching one Galaxy III; RCA Americom Inc. for five satellites plus one in-orbit spare; Satellite Business Systems Inc. for two launches; Southern Pacific Satellite Co. for one launch plus a ground spare, and Western Union Corp. for launching Westar VI. Conditional authorizations went to Advanced Business Communications Inc., Rainbow Satellite Inc., and United States Satellite Systems Inc., for two launches and one ground spare each.

. . . as NASA seeks ways to pack more into orbit

Making room for the new orbital entries is a recent FCC authorization for as little as 2° spacing between domestic satellites operating in the 12- and 14-GHz and 4- and 6-GHz bands by 1986. But the action **will only temporarily delay the saturation of the geosynchronous orbital arc,** which, according to a study sponsored by NASA's Lewis Research Center of Cleveland, can accommodate only some 1,400 to 1,500 36-MHz transponders—a limit that will be reached by the early 1990s. The problem has Lewis researchers cooperating with industry on developing multiple spot-beam antennas and digital switching systems to permit 1° spacing of satellites, with more communications channels in the 20-to-30-GHz range.

RCA has lowest TV noise figure says FCC study

The uhf noise figure of RCA's television sets leads a list just released by the Federal Communications Commission in an analysis of noise data supplied by 17 domestic and foreign TV manufacturers. The report says that tuners produced by the RCA Consumer Electronics division in Indianapolis have a mean noise figure of 8.02 dB compared with the industry mean of 8.9 dB and the FCC-mandated standard of 12 dB. Jim Cochran, director of the RCA division's signal systems and components operation, attributes the achievement to both **solid-state improvements in tuning diodes and rf devices and more stringent quality-control measures.** RCA has 20% of the U. S. market of 10 million sets a year.

Defense, Energy groups to study supercomputers

A three-level Federal study effort on supercomputers is being set up in the Departments of Energy and Defense at the direction of the White House. The Energy Department's Office of Energy Research will examine how **the Government's own supercomputer needs can be used to encourage the two U. S. producers—Control Data Corp. and Cray Research Co.—to continue development.** The second, a combined Energy-Defense group, will look at ways of making supercomputers more accessible to qualified U. S. researchers. The third, the Defense Advanced Research Projects Agency, will promote the exchange of data in such areas as artificial intelligence and supercomputer architecture and software.

Circle 69 on reader service card

Washington commentary

U. S. technology and trade: the need for data

Trade is not always at the forefront of the minds of America's technologists, most often seen as too busy measuring nanoseconds to care about megabucks. It is an old criticism in Washington, which has long faulted engineers and scientists in academia and industry for failing to keep up with developments abroad. It is also a criticism loaded with irony, given that it comes from a government that, unlike most others, provides no central support for one of the most inexpensive and productive forms of intelligence gathering: monitoring, translating, and distributing in timely fashion the technical papers and related market data published in other countries.

The grossness of that governmental failure to set up a central data bank on technological developments abroad stands in sharp contrast to the superficiality of Washington's own most recent proposal for keeping U. S. companies competitive in their own markets and those overseas. The Reagan Administration wants to create a new Department of Trade, lumping together the U. S. Trade Representative's office and most of the Department of Commerce—the National Bureau of Standards, the Census Bureau, the Patent Office, the International Trade Administration, and the Office of Telecommunications Policy, among others.

Power struggles

Many trade specialists in and out of Government question how much good such a reorganization and consolidation will accomplish. To one insider, the Department of Trade shapes up as "a poor carbon copy of MITI," Japan's Ministry of International Trade and Industry, "that is not suited to our [American] style." A skeptical electronics exporter suspects the reshuffle will leave him "doing business with the same old bureaucracy wearing new titles." Sen. William V. Roth, the conservative Delaware Republican, concurs with the latter view in his call for a new "lean and mean" trade organization.

Bureaucratic turf fights compound the problems of organizing the Department of Trade. The Department of Defense, for example, is lobbying hard to extend its veto rights over technology exports. Whereas the Pentagon's export control power is now limited to licenses sought for shipments to the Communist Bloc nations, it is pushing to have that veto right extended to shipments to U. S. allies and neutrals. At the same time, the State Department wants to retain its power to deny exports to nations that may, at any given time, be present on its list of political unfriendlies.

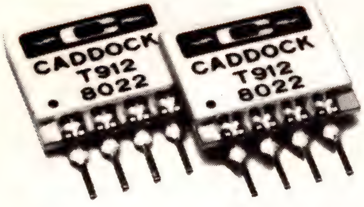
High-technology exporters, especially U. S. multinationals dealing in areas like computers and communications, are troubled by the struggle. "It's going to be a tough fight with a lot of bloodletting," says one trader. "I still wonder if the country is going to be better for it."

The information gap

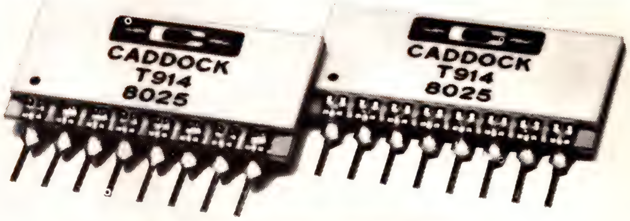
If the Department of Commerce is reorganized to become the Department of Trade, however, the change will benefit none of those it is designed to serve unless it includes a central system for timely collection and distribution of data on foreign technology and overseas markets. Such an effort admittedly may not help the U. S. recapture the 90% share of its own market for manufactured goods that it held some 25 years ago. But a well-developed program, properly exploited by American growth industries like electronics, could not only prevent U. S. manufacturers from losing any more than the 50% share of their home market that they still hold, but could also expand the U. S. share of new markets developing abroad—markets already being targeted by America's competitors.

Coupling such a mechanism to another for providing growth industries with access to domestic capital could do far more for their expansion and exports than simply reshuffling the Washington bureaucracy. The costs of capital, its use and abuse by industry, will be considered next in this column. **–Ray Connolly**

Type T912 / T914 Ultra-Precision Resistor Networks from CADDOCK provide Ratio TCs to 2 PPM/°C and Ratio Tolerances to ±0.01% for precision analog designs.



Type T912 Ultra-Precision Resistor Network 'Pairs'

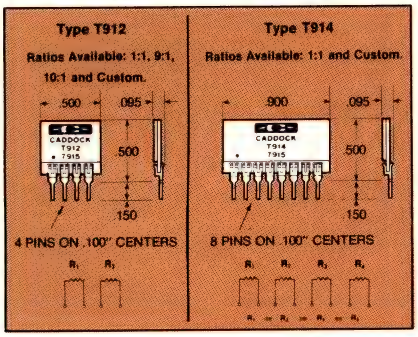


Type T914 Ultra-Precision Resistor Network 'Quads'

Type T912 / T914 Ultra-Precision Resistor Networks are constructed with Caddock's Tetrinox™ resistance films to achieve all of these high performance characteristics:

- **Absolute Tolerance:** 0.1% for all resistors.
- **Ratio Tolerances:** From ±0.1% to ±0.01%.
- **Ratio Temperature Coefficients:** From 10 PPM/°C to 2 PPM/°C.
- **Absolute Temperature Coefficient:** ±25 PPM/°C from 0°C to +70°C, referenced to +25°C.
- **Ratio Stability of Resistance at Full Load for 2000 Hours:** Within ±0.01%.
- **Shelf Life Stability of Ratio for Six Months:** Within ±0.005%.

This exceptional combination of performance specifications – and the compact, plug-in configuration of the Type T912/T914 precision resistor 'pairs' and 'quads' – provide the single-package matched resistor characteristics and stability required by high-accuracy analog circuits, including –



- **Precision analog amplifiers.**
- **Voltage reference circuits.**
- **Instrumentation bridge circuits.**
- **Voltage and current comparison circuits.**

Standard models of Type T912 / T914 precision resistor 'pairs' and 'quads' include 14 off-the-shelf resistor values with a wide choice of Ratio Tolerances, Ratio TCs and Resistance Ratios:

This standard part number provides a selection of over 500 in-production models of Type T912/T914 precision resistor 'pairs' and 'quads':

T912 - A 1K - 010 - 10

Model Number:

Ratio Code Letter:

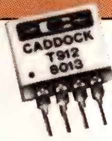
A – T912 with $R_2 = 10R_1$
(Example: 1K – 10K)
B – T912 with $R_2 = 9R_1$
(Example: 1K – 9K)
No Letter – T912 with $R_2 = R_1$
No Letter – T914 with $R_1 = R_2 = R_3 = R_4$

Ratio Temperature Track: (0°C to +70°C)
-10 = 10PPM/°C
-05 = 5PPM/°C
-02 = 2PPM/°C

Ratio Tolerance:
-100 = 0.1%
-020 = 0.02%
-050 = 0.05%
-010 = 0.01%

Standard Resistance Values (R_1):

1K	10K	40K	200K	500K
2K	20K	50K	250K	1 Meg.
5K	25K	100K	400K	



As an example of the price/performance advantages of this advanced resistor technology, the Model T912-A1K-010-10 shown here provides a 1K-10K resistor 'pair' with a ratio tolerance of ±0.01% and a ratio temperature coefficient of 10 PPM/°C at a 1000-lot unit price under $2.55. The same resistor 'pair' with a ratio tolerance of ±0.1% delivers at a 1000-lot unit price under $1.50!

Type T1794 Custom Precision Resistor Networks meet special circuit and packaging requirements:

For medium- to high-volume applications, Type T1794 resistor networks provide all of the standard Type T912/T914 specifications, plus –

- From 2 to 15 resistors per assembly.
- Absolute tolerances from 1.0% to 0.01%.
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- Resistance values from 500 ohms to 10 Megohms
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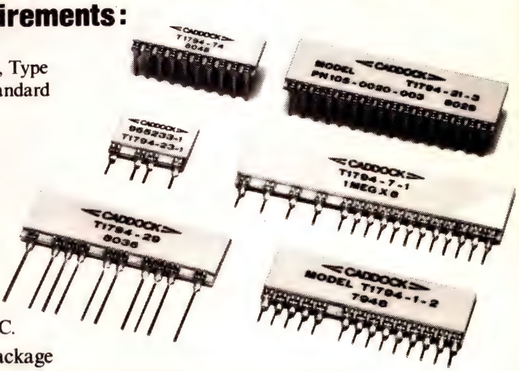

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Discover how easily these problem-solving resistors can improve the performance and reliability of your equipment, too. For your copy of the latest edition of the Caddock 24 page General Catalog, and specific technical data on any of the more than 150 models of the 13 standard types of Caddock High Performance Film Resistors and Precision Resistor Networks, just call or write to –

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7200 A The above all lab generator by its multiple possibilities and its performance level.

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- SSB noise at 6.25 KHz: − 136 dB/Hz,
- SSB floor noise: − 150 dB/Hz,
- modulations AM/FM/PM/pulse (=, ∿),
- AF programmable generator: 10 Hz to 100 KHz.

740 A
- 0.1 to 1120 MHz by 10 Hz steps,
- floor noise: ⩽ − 140 dB/Hz,
- modulations: AM/FM/PM/pulse,
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- auxiliary RF output,
- 40 complete settings non volatile memories,
- RF leak: ⩽ 1μ V,
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7200 A
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- **moreover, a powerful firmware**

Uallows an exceptional accuracy:
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- **of the modulations: 2%,**
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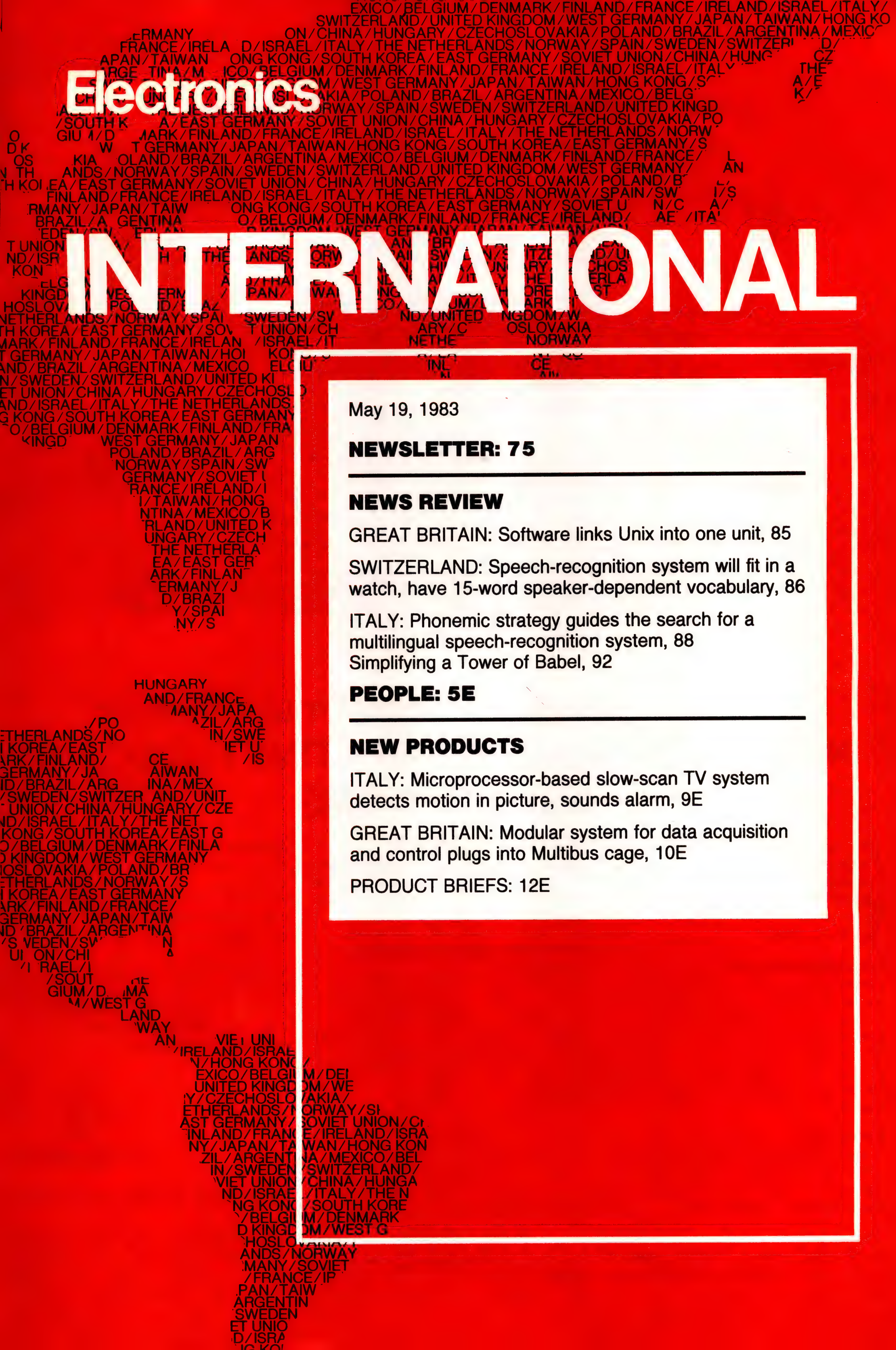

May 19, 1983

NEWSLETTER: 75

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GREAT BRITAIN: Modular system for data acquisition and control plugs into Multibus cage, 10E

PRODUCT BRIEFS: 12E

Two low-priced universal instruments: NORMA Messtechnik's MULTIMETER D 3210 and D 3230 RMS

The new MULTIMETERS D 3210 and D 3230 RMS are universal and reliable instruments. 10,000 resp. 2,000 hours of battery life ensure readiness of operation at all times – and they are sensationally low-priced.

Comprehensive ranges
Electronics and electrical engineering make increasing demands on meter ranges. The MULTIMETERS D 3210 and D 3230 RMS will measure currents up to 20 A, voltages up to 2000 V and resistances up to 20 megohms. A continuity tester with acoustical signal is also available.

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NORMA Messtechnik's successful multimeters

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	2 mA–10 A	200 mV– 750 V	
D 2210	20 nA–200 mA	200 mV– 600 V	2 kΩ–2 MΩ
	2 mA–200 mA	200 mV– 600 V	
D 2230	20 nA–200 mA	200 mV– 600 V	2 kΩ–2 MΩ
	2 mA–200 mA	200 mV– 600 V	
D 3210	200 μA–20 A	200 mV–2000 V	200 Ω–20 MΩ
	200 μA–20 A	200 mV–2000 V	
D 3230 RMS	200 μA–20 A	200 mV–2000 V	200 Ω–20 MΩ
	200 μA–20 A	200 mV–2000 V	
DA 3232	200 μA–20 A	200 mV–(2000 V)	200 Ω–20 MΩ
	200 μA–20 A	200 mV–(2000 V)	
D 4025	250 μA–2,5 A	250 mV–1000 V	25 Ω–25 MΩ
	250 μA–2,5 A	250 mV–1000 V	
D 4045 IEC 625	250 μA–2,5 A	250 mV–1000 V	25 Ω–25 MΩ
	250 μA–2,5 A	250 mV–1000 V	

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International newsletter

West Europe's Esprit plan moves toward approval . . .

Government and private sources concerned with the future of the West European electronics industry have come up with a host of plans and studies in the uphill battle to regain territory lost to the U. S. and Japan. Playing catch-up, the European Commission hopes to approve by November its proposed $1.5 billion research program in information technologies. The commission this week will ask EC governments to approve $750 million in funding as their share of the five-year matching-grant scheme known formally as the European Strategic Program for Research in Information Technologies (Esprit) [*Electronics,* Aug. 25, 1982, p. 85]. The EC will come up with the other $750 million. **Approval this fall would permit the commission staff to start awarding initial projects in 1984.** Also starting after earlier funding delays is an $80 million matching-grant program for research in very large-scale integrated-circuit production technology and computer-aided design.

Commission sources expect the private electronics sector to back Esprit, but passage will depend on the willingness of national governments, many of which are funding their own programs, to approve extra spending at the European level. Some EC experts predict West Germany and the UK will support the proposal; the reaction of France, whose electronics industry is in the course of nationalization, is unsure.

. . . but will it stop the semiconductor industry's slide . . .

The West European semiconductor market is heading for a solid 13% growth in 1983, says market researcher Dataquest UK Ltd. of London. As in 1982, the first quarter was strong, but unlike last year, **the 23% to 25% growth over the fourth quarter of 1982 should presage a true upturn,** for the growth is real, if fragile, and not just restocking, says the company. It warns, however, that West European manufacturers' share of the total world semiconductor market is still sliding—from 15% in 1977 to 11% in 1982—which could hurt not only the companies themselves but Europe's ability to contend on an international level. Also, if the U. S. Department of Defense goes ahead as planned to restrict the export of chip technology, Europe's hopes of competing seriously in advanced semiconductor markets might be further dashed, says Dataquest. It adds that Esprit is attracting European support, but whether nationalistic sentiments can be overcome remains to be seen.

. . . without a more novel joint-venture approach . . .

A new venture that combines local governmental and private assistance to one troubled electronics firm may provide an alternative pattern of survival for the European electronics industry, say those involved. The aim of starting an "Italy Inc." and later a "Europe Inc." in electronic products is **to better use capacity and, by being more cost-competitive, contain inroads being made into the industry by Japanese competitors.** The troubled company slated for assistance is the Zanussi Group of Pordenone, Italy, whose consumer electronics business lost $12.86 million last year. Capital for the venture will come from an electronics holding company, Rel, which the Italian Ministry of Industry is now setting up. Market know-how is to come from private companies, and to this end Rel has contracted Dutch manufacturer NV Philips Gloeilampenfabrieken to provide technological and marketing know-how to Zanussi, largely in color TV. After Zanussi, Rel will finance a series of joint ventures with private electronics producers. Final details are yet to be set; the entrance of other partners into the Zanussi-Rel-Philips venture, such as Italy's equally troubled Indesit and France's Thomson-Brandt, has not been ruled out.

. . . or is even the fifth-generation computer beyond Europe's reach?

In the race for functional fifth-generation computers, the U. S. and West Europe lag far behind the Japanese, and Esprit will not help, implies an analysis prepared by the German Economics Institute. The Cologne, West Germany, organization predicts that Japanese industry will have the knowledge-based computers ready for international markets by the mid-1990s. In West Europe and the U. S., by contrast, none of the fifth-generation projects under way are as all-encompassing and capital-intensive as the Japanese one. In particular, the institute, like the European Community, **doubts that the European research and development activities are at a high enough level to catch up,** and it deems the various countries' efforts too splintered to achieve the solidarity needed. What is called for, the institute says, is a data-processing– and communications-related research project that far transcends Esprit.

Single-unit VCR uses standard tape

Starting July 21 in Japan, Sony Corp. will be selling a single-unit Beta-format video-cassette recorder and color camera that have been shoehorned into a small package weighing only 2.48 kg. The Betamovie records on standard cassettes for up to four hours in the Beta II mode. **Key to the design shrink is a head drum about three fifths the diameter of those in standard Beta units.** The tape is wrapped 300° around the drum rather than 180°, and the camera tube's scan is speeded up to finish in five sixths of the usual time. Also contributing to the small size is a ½-in. color vidicon tube, replacing the 2/3-in. tube typical in consumer color cameras. Price in Japan will be $1,165. U. S. and European versions might be available late this year at a price yet undecided.

Chip integrates all three color-TV output stages

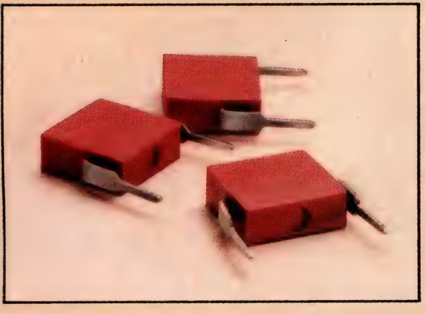
With a new junction-isolation technology that can withstand a collector-source voltage of more than 300 V, SGS-Ates Componenti Elettronici SpA has integrated on a single chip all three video output stages necessary to drive the cathodes of a color TV tube. With a double-diffusion process wherein boron is implanted from below through the p^+ buried layer and from above by normal predeposition, the Agrate, Italy, company preserves as much as half of the essential epitaxial layer lost in standard diffusion from above—the principal determining factor for breakdown voltage. **The 7,300-mil^2 power-stage chip realized with the technology boasts a 200-V supply, a 6-MHz bandwidth, a slew rate of 1,000 V/ms, and an output load of 15 pF.** In addition, SGS claims the chip is remarkably reliable, having operated for 1,000 hours at 150°C.

Addenda

As part of its complete reorganization, CII-Honeywell Bull of Paris (see p. 107) will **change its name to, simply, Bull,** and its charter to that of a holding company that includes overall administration and a single sales force for four principal subsidiaries and profit centers. . . . Sweden and Norway have finally given a go-ahead to **an experimental Scandinavian telecommunications satellite** after more than five years of studies and negotiations. Tele-X, to be launched in 1986 by an Ariane missile, will contain two TV channels and two data-video channels.

New laser technology shrinks TRW 80 Series film capacitors to ceramic size.

Small Wonder.



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Introducing TRW's new Micro Thin Gauge Series 80 capacitor. A cost-effective way to improve products and flatten the failure curve.

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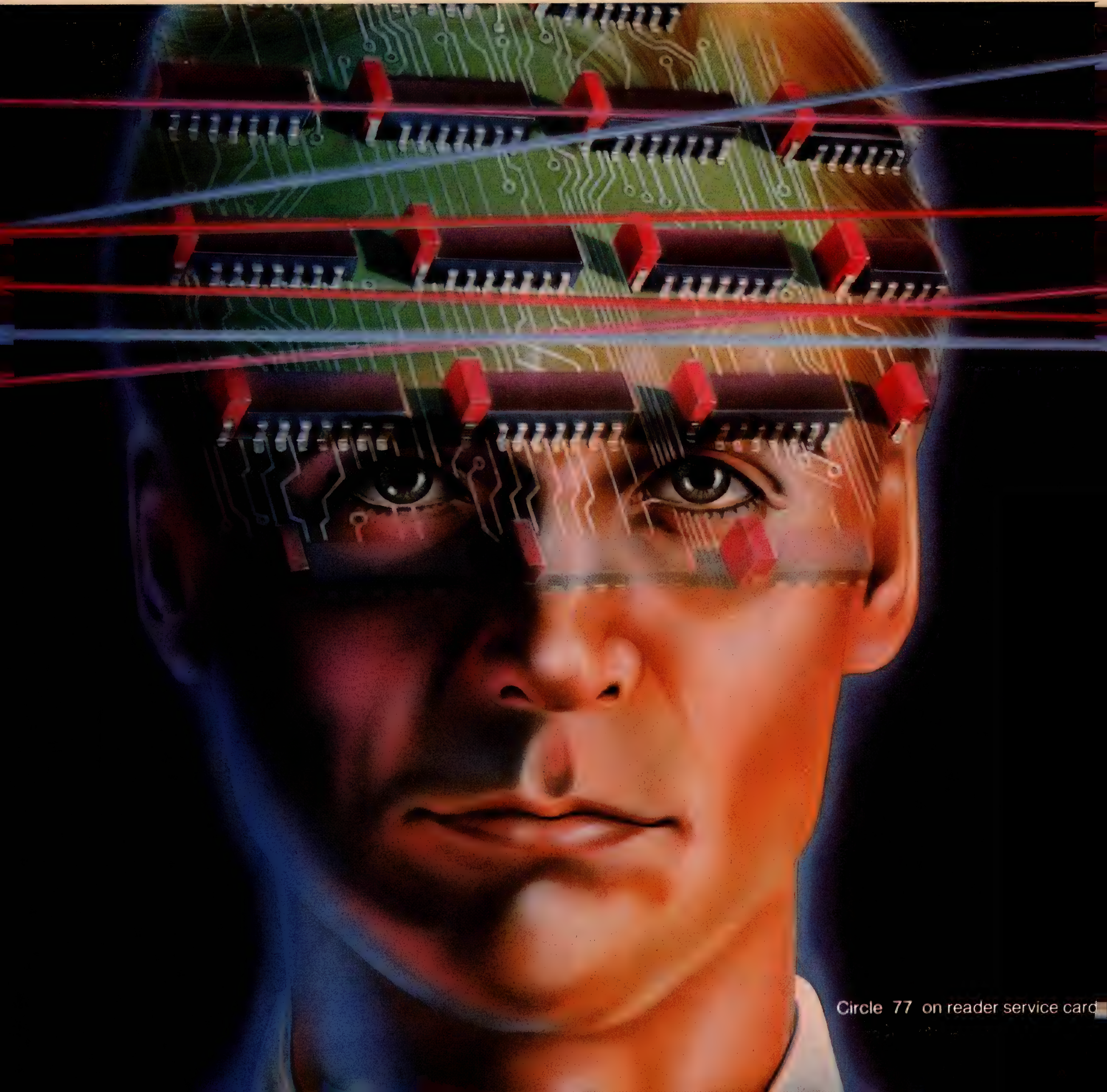

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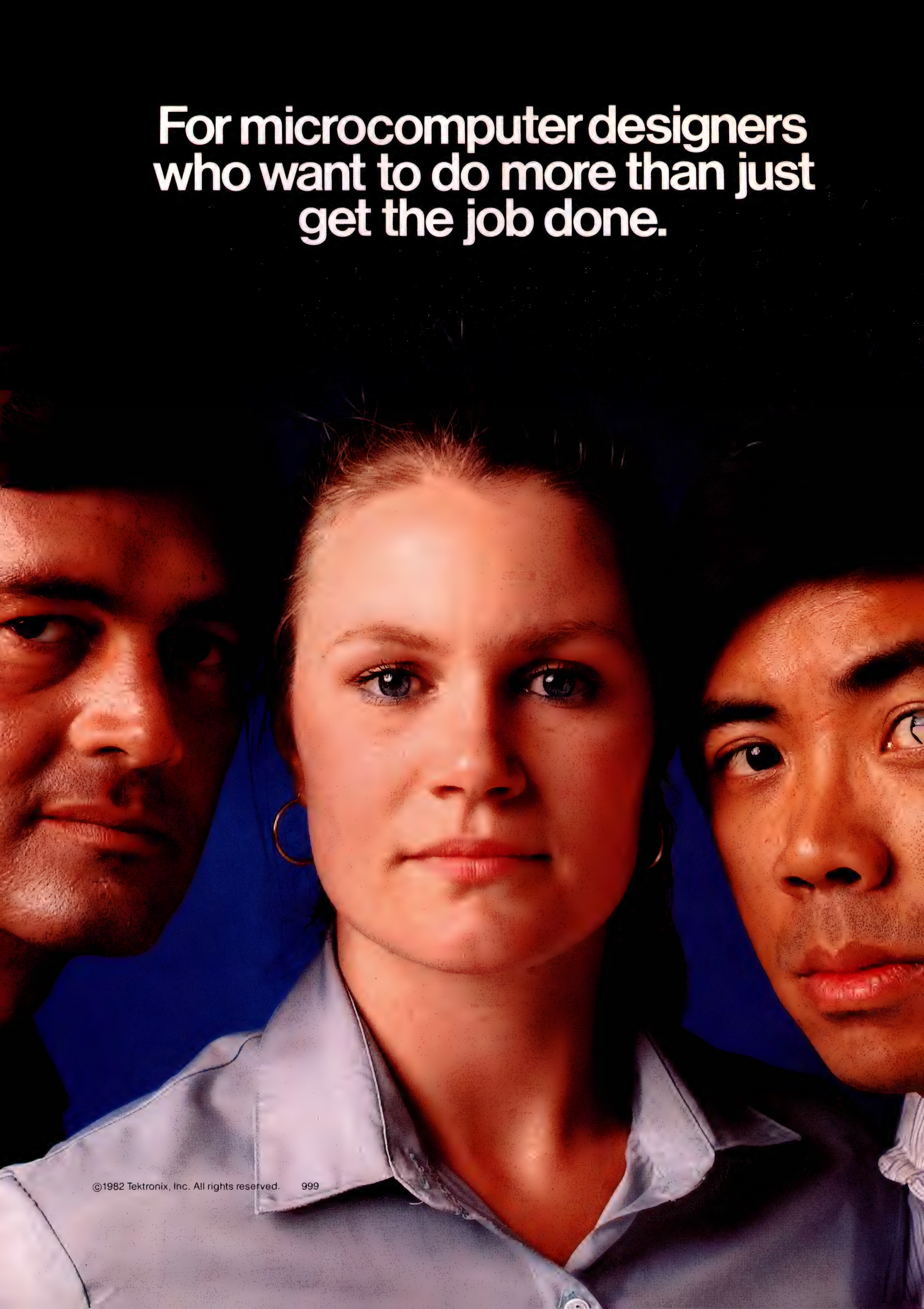
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Develop software on host computer.	Single users develop software with 8500 Series tools running under 8550's DOS/50, with an advanced hierarchical filing system and a friendly user interface.	Multiple users develop software with 8500 Series tools running under 8560's TNIX, a derivation of Bell Laboratories' UNIX** Operating System.
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Real-time debugging with Trigger Trace Analyzer. Up to ¼ Mbyte emulation memory.	Real-time debugging with Trigger Trace Analyzer. Up to ¼ Mbyte emulation memory.	Real-Time debugging with 8540's Trigger Trace Analyzer.

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TMS9900	Z80A	8039	3874
SBP9900	8080A	8039-A	3876
	8085A	8035	F-8
	8049	8021	

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For real-time debugging, the Trigger Trace Analyzer.

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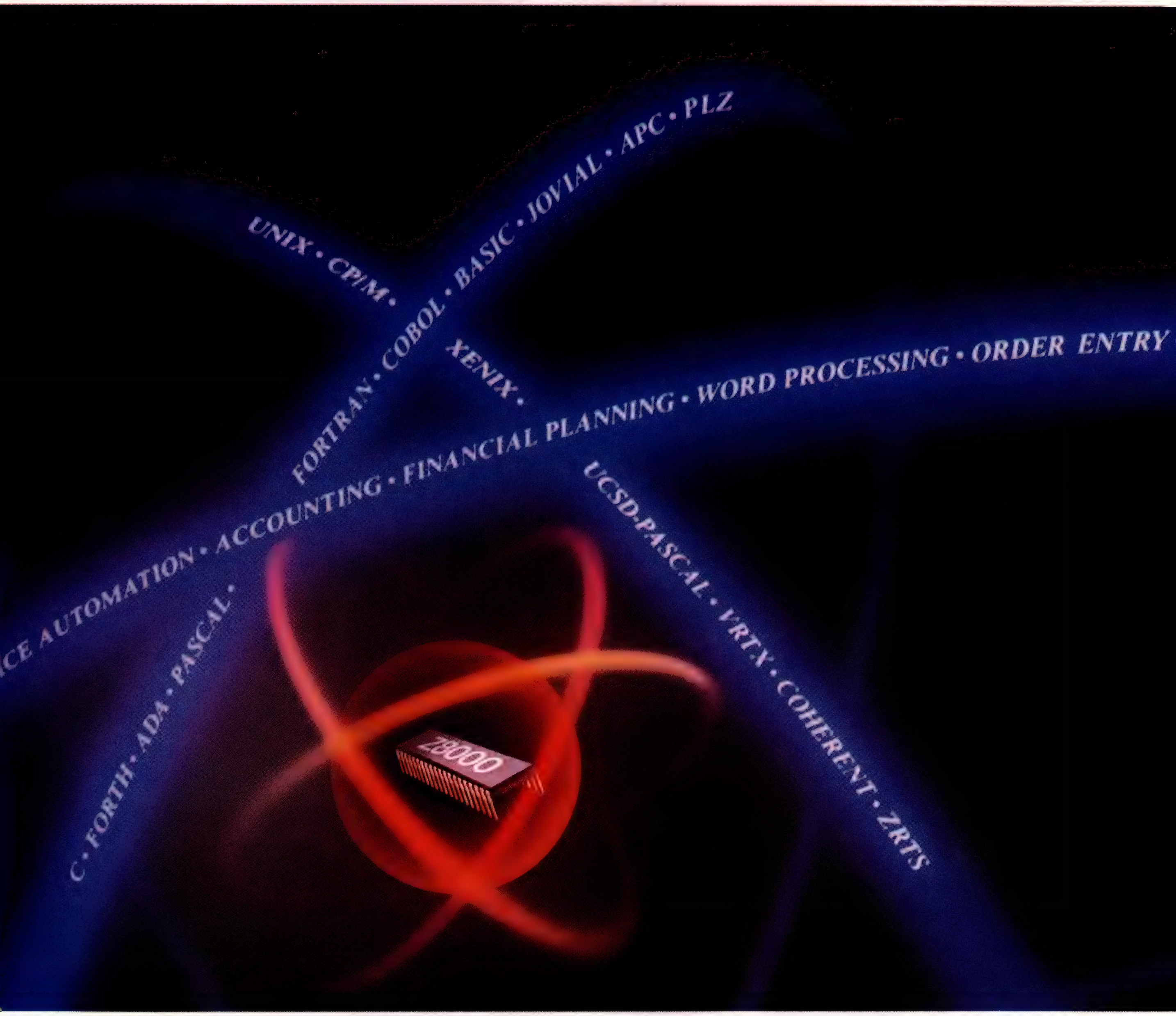
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Electronics international

Significant developments in technology and business

Software links Unix systems into one unit

by Kevin Smith, Senior Editor

A hierarchical naming structure makes each system behave as if it were a super directory under control from the top

The world of open systems interconnection, in which different manufacturers' computers can freely exchange data, programs, and files, may still be a long way off. But for users of Bell Laboratories' Unix operating system, it could be just around a Newcastle corner.

At the University of Newcastle's Computing Laboratory, a group of researchers under Brian Randell has developed a software package called the Newcastle Connection that can make a network of different computers all running Unix behave like a single machine. At the user and program level, such a network is functionally equivalent to a conventional single-processor Unix system.

Structures joined. In fact, the resulting distributed system is functionally indistinguishable at both the user-interface and system-call levels from a single central Unix system. The secret of success is the hierarchical naming structure for directories, files, devices, and commands.

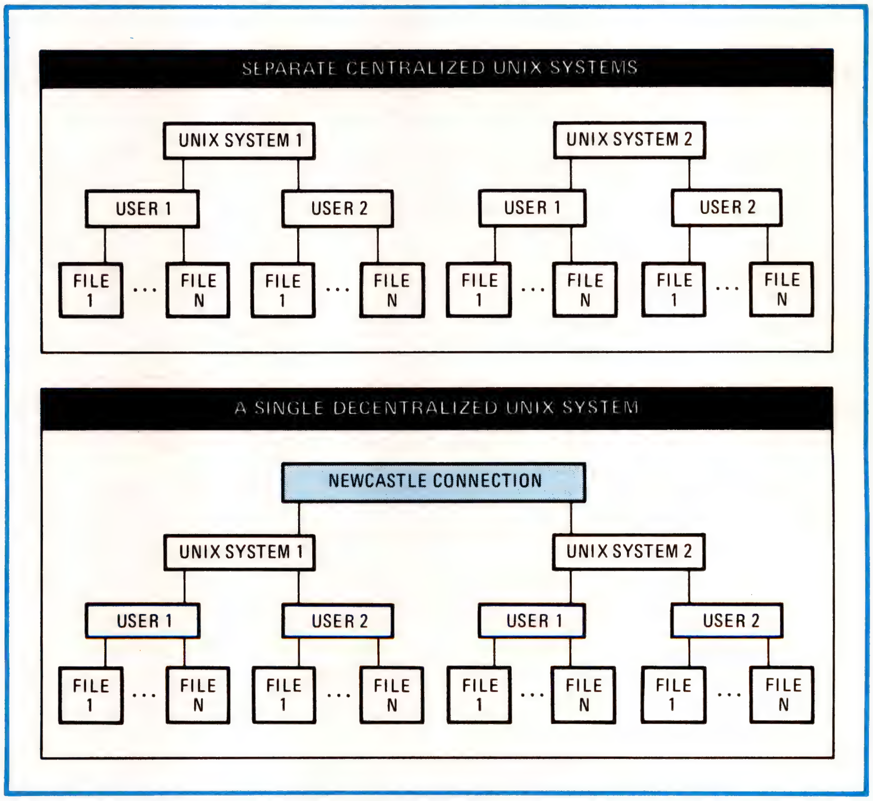
The various Unix systems are connected as a single structure in which each system behaves as a super directory under the Newcastle Connection at the top of the hierarchy. Issue 1 of the Newcastle Connection is for single networks. It will be followed within months by Issue 2, for communication between networks.

So far there is only one prototype up and running—a network of five PDP-11s connected by a Cambridge ring. However, the Newcastle software has aroused tremendous industrial interest.

In Unix, all user processes and many operating-system facilities interact with each other and the outside world by means of procedure calls on the resident nucleus of the operating system. The Newcastle Connection is a transparent software layer that is inserted between the kernel and these processes.

Its role is to filter out calls that have to be redirected from one Unix system to another because they cover files or devices on the latter. Also, it accepts calls that have been redirected from one system to another. Each component Unix system stores just the part of the overall naming structure representing its own section of the naming tree. Access to other files and other parts of the system can thus be transparent to the user.

Orders for the software, to be mar-



Traffic cop. With the Newcastle Connection acting as a supervisor at the top of a hierarchy of Unix systems, any user can access files on any system in the hierarchy, as if they were on his own system. Appropriate global access protections are administered by the Newcastle Connection communications software. Hierarchical addressing becomes a sequence of selections, similar to international telephone dialing.

keted through the Microelectronics Application Research Institute (MARI) in Newcastle-on-Tyne, already top $1 million, with companies like Digital Equipment Corp. and Tandberg Data A/S signed up, and others, for example Logica Ltd., in advanced negotiation.

ICL plc, too, has evaluated the software for implementation on its high-performance single-user work station, Perq. Clothed in a Unix operating system, Perq has already been selected by Britain's Science and Engineering Research Council as its standard workhorse.

In addition, researchers engaged in Britain's newly authorized fifth-generation–computer research program [*Electronics*, May 5, p. 76], could well communicate with each other through the Newcastle Connection, since the program is also standardizing on Unix.

Hardware advantage. MARI marketing manager Paul Robinson says the Unix kernel is standard—the Newcastle Connection sits on top of it without any internal tinkering. Also, the Connection software is hardware-independent, a big advantage over a rival commercial system from Plexus Computers Inc. that is designed to operate on the Santa Clara, Calif., computer company's own hardware.

Although there is a growing list of companies talking to Robinson, some still have reservations. ICL, for one, says the connection is of limited application because it does not conform to the seven-layer reference model for open systems interconnection that has been worked out by the International Standards Organization.

Randell concedes the point: the Connection "hides the bottom four layers from the user and in a sense does away with the need for the other three, substituting for them the full Unix system-call interface.

"The seven-layer model is an abstract operating system whose merits can't be proved till mapped onto a real-life operating system," he adds. "Unix, by contrast, is a modern operating system already implemented on a wide and ever-growing variety of different hardware."

Also, Unix has features that make it ideal for parallel processing and distributed systems, says Randell. One such is its file-store management structure. It comprises a hierarchy of variously sized files and directories. Files can be retrieved by being addressed contextually, rather than by being named.

This contextual addressing capability, it turns out, is an extremely powerful and liberating concept. It releases memory from the limitations of a machine's address space. Instead, addressing becomes a sequence of selections much like dialing the international, country, city, and area code, exchange, and number of the telephone network. "What's needed is a global address space, not a global memory," is the way one Newcastle researcher puts it.

Transparent operation. Usually the hierarchical Unix file structure resides on a single machine. Newcastle's contribution is to show that a user can move between file structures on different machines transparently.

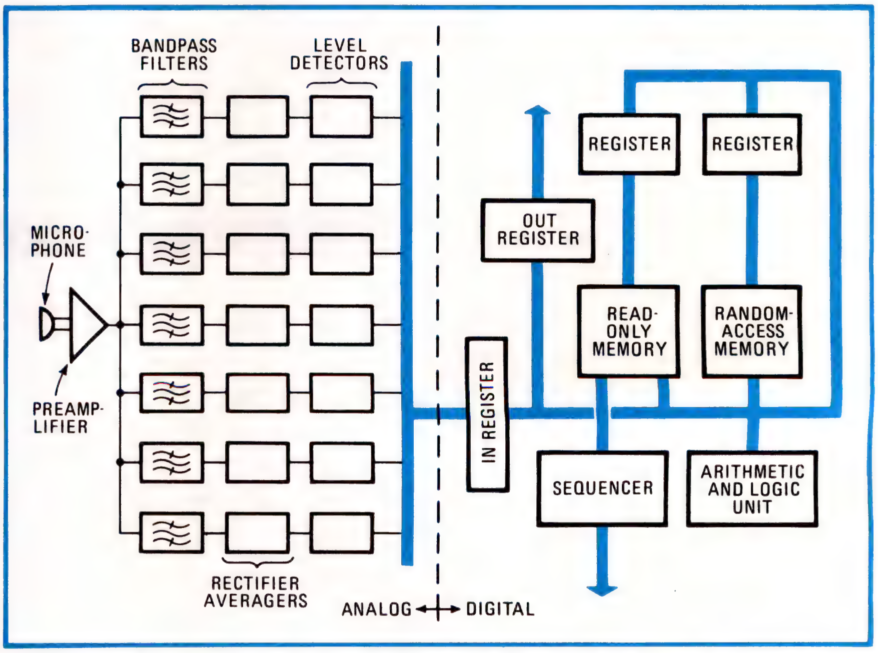
Further developments in the pipeline will provide multilevel security and hardware fault tolerance. Prototype systems have already been built.

Switzerland

Speech-recognition system fits in watch, responds to five one-word commands

Minimal power consumption and small size combine in a novel speech-recognition system now in development at Asulab AG in Neuchatel, Switzerland. These attributes, plus the low cost of the final chip, will make the system applicable in battery-powered consumer products like watches, clocks and toys, as well as remote-control units for home appliances and radio and TV sets.

Sporting a 15-word vocabulary, the system currently under development for watches will recognize 10 spoken digits and five one-word commands. Its 1,500-bit memory is small



Two-parter. Asulab's voice-recognition chip has an analog and a digital part, the latter implemented as a custom-designed microprocessor. To store the significant features of its 15-word vocabulary in a random-access memory 10 mm^2 in area and holding 100 b/mm^2, both digital and analog techniques of signal processing had to be used.

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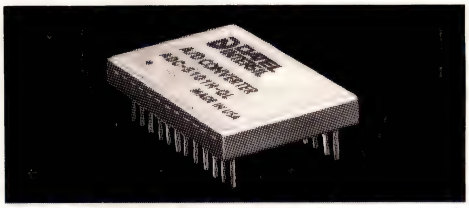

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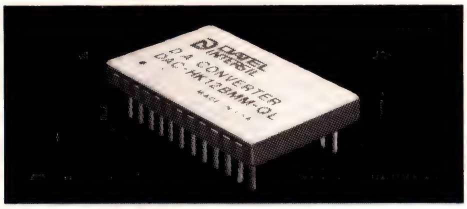

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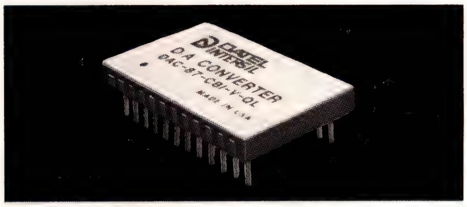

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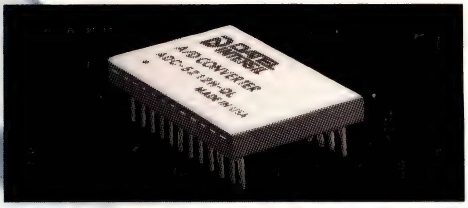

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enough for low-volume and inexpensive chip implementation, yet large enough to completely program a watch or, for that matter, other equipment around the house.

Watch commands. With the system integrated into a wrist watch, for example, the user may give the voice command "alarm" followed by four digits such as zero, six, zero, zero. That sequence programs the watch to sound an alarm at 6 a. m.

Besides the alarm function, the system has four others: a stop-watch function, a dual-time mode that indicates the time in another city, a timer mode that implements a countdown time function, and the standard time-indicating function.

The Swiss system is speaker-dependent—that is, it responds to one particular voice. However, if another person simply repeats a word several times, the system adapts itself to that person's voice—or language. Word-recognition accuracy is typically 95%, comparable with that of currently available high-cost systems.

Asulab, the research and development laboratory for the Swiss watchmaking group Asuag AG, is completing its development, aiming for commercial applications in the near future. "Under a nonexclusive contract, one company has been licensed to use the system, and others may follow suit," says Friedrich K. von Willisen, director of Asulab.

When fully integrated, the silicon-gate complementary-MOS chip will be about 40 square millimeters in size (including the memory) and consume typically 200 microwatts at 3 volts. The input device is a tiny electret microphone housed in a 3-by-5-mm package. The system is immune to background noise.

Storing restriction. The most restrictive factor in designing a speaker-dependent system is the capacity of the random-access memory for storing the voice characteristics of the words spoken. Given a RAM density of about 100 bits per square millimeter, "both analog and digital techniques must be applied to signal processing to extract significant features and store a 15-word vocabulary in a RAM area of 10 mm^2," explains project leader Ngoc C. Bui.

Unlike other systems, the Asulab chip uses virtually no peripheral devices. It comprises an analog preprocessor and a special microprocessor (see figure), both Asulab-designed. After preamplifying the acoustic signal from the external microphone, the preprocessor analyzes that signal within a 200-to-4,500-hertz range, breaking it down into seven channels by means of bandpass filters.

Once the signal from each channel is rectified and averaged, its energy is extracted and digitized with a variable threshold that tracks the level of the input acoustic signal. Sampling every 10 milliseconds yields a data rate of 700 bits per second at the parallel outputs, implemented as a seven-line data bus.

To keep power consumption low, all circuits used in signal analysis, such as the fourth-order bandpass filters and the energy extractors, are designed in low-power switched-capacitor technology, points out Bui. The bandpass filters are realized by cascading two second-order sections.

Further signal processing is done in the microprocessor. It eliminates redundancy in the voice signal and codes and compresses the 700-b/s data stream from the preprocessor by using run-length coding, popular in image processing.

Then, in the recognition mode, the microprocessor goes through the correlation process according to a program stored in its 10-K read-only memory. This process entails comparing the characteristics of the incoming word with the sonogram of the word stored in the RAM.

At a clock rate of 32 kilohertz, a common value for electronic watches, it takes only about 100 milliseconds to perform a correlation, this short time being a result of a well-defined instruction set. (Speech recognition systems already on the market also feature 100-ms correlation times, but at clock rates much higher than 32 kHz, Bui says.) The microprocessor's sequencer handles system timing, and its arithmetic and logic unit performs functions like estimating the similarity of input and reference words.

Thus far the Swiss engineers have integrated the switched-capacitor filter banks, the level detectors for analog preprocessing, the ALU, the sequencer, and the RAM. The software and all critical parts of the hardware have been extensively tested.

At this point, Asulab director von Willisen is reluctant to give information on chip prices. But he hints that, given the small silicon area and the relatively small vocabulary, the cost will be fairly low. **–John Gosch**

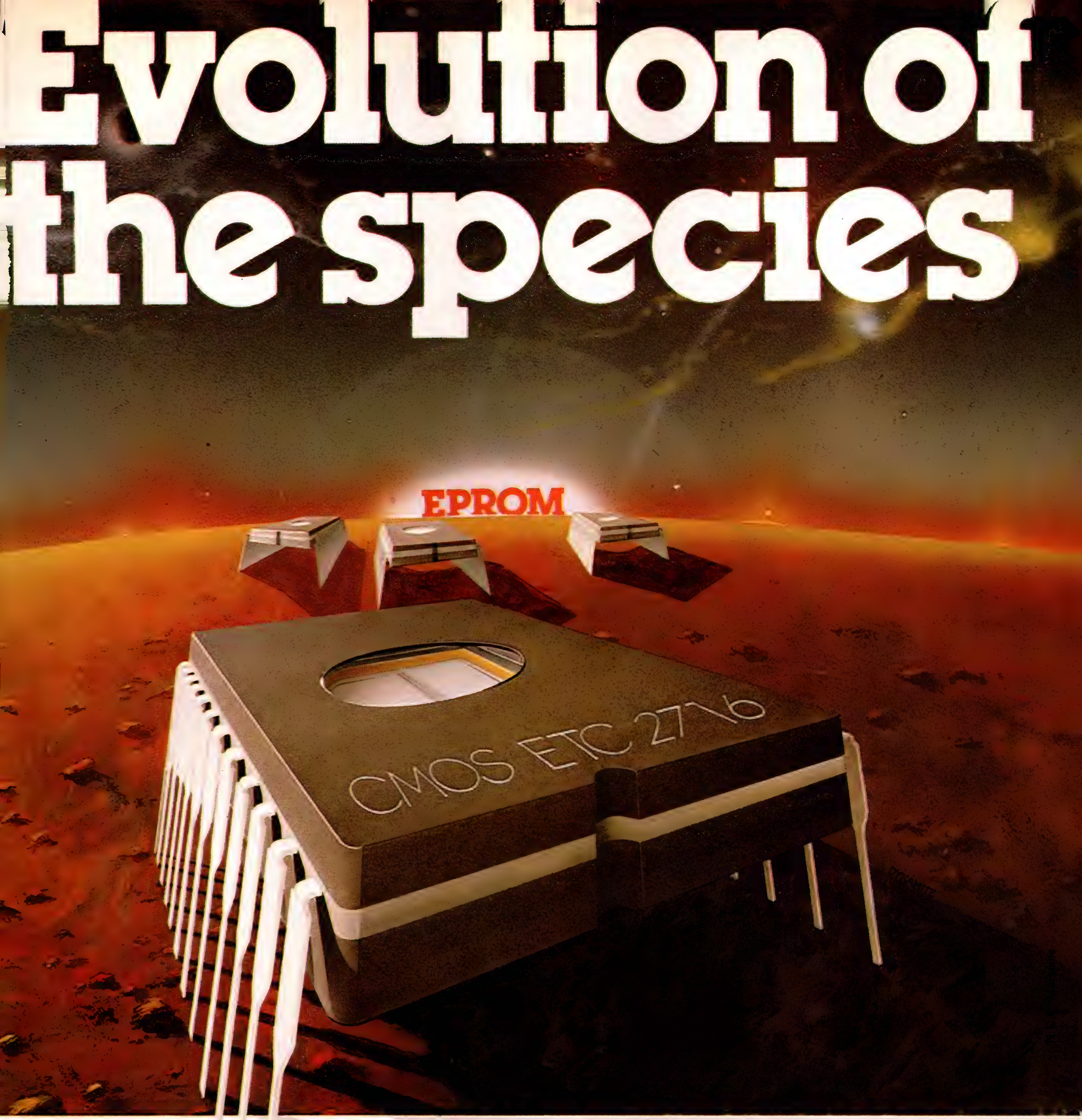
Italy

Phonemic strategy guides the search for multilingual speech-recognition system

To meet the needs of its multilingual clientele, Ing. C. Olivetti & Co. is working on a speech-recognition system based on the phoneme, the smallest unit of speech. The Ivrea, Italy, company feels this will lead to a cost-effective solution in Spanish, English, French, and German, as well as Italian, with favorable compromises on speaker dependence, dictionary size, and continuous speech—the principal characteristics defining the value of such a system.

"In the end, everyone has the same theoretical objective: to design a speaker-independent system that recognizes continuous speech using an unlimited dictionary with no syntax constraints," points out Vittore Vittorelli, Olivetti's voice processing manager at the Technology Research Center in Ivrea. "Essentially, this means that, in a normal conversational situation, the listener would be replaced by a machine.

"A full emulation of this process would probably, at the moment, be impossible and certainly too costly for the industrial applications of Olivetti, but there is no reason why the



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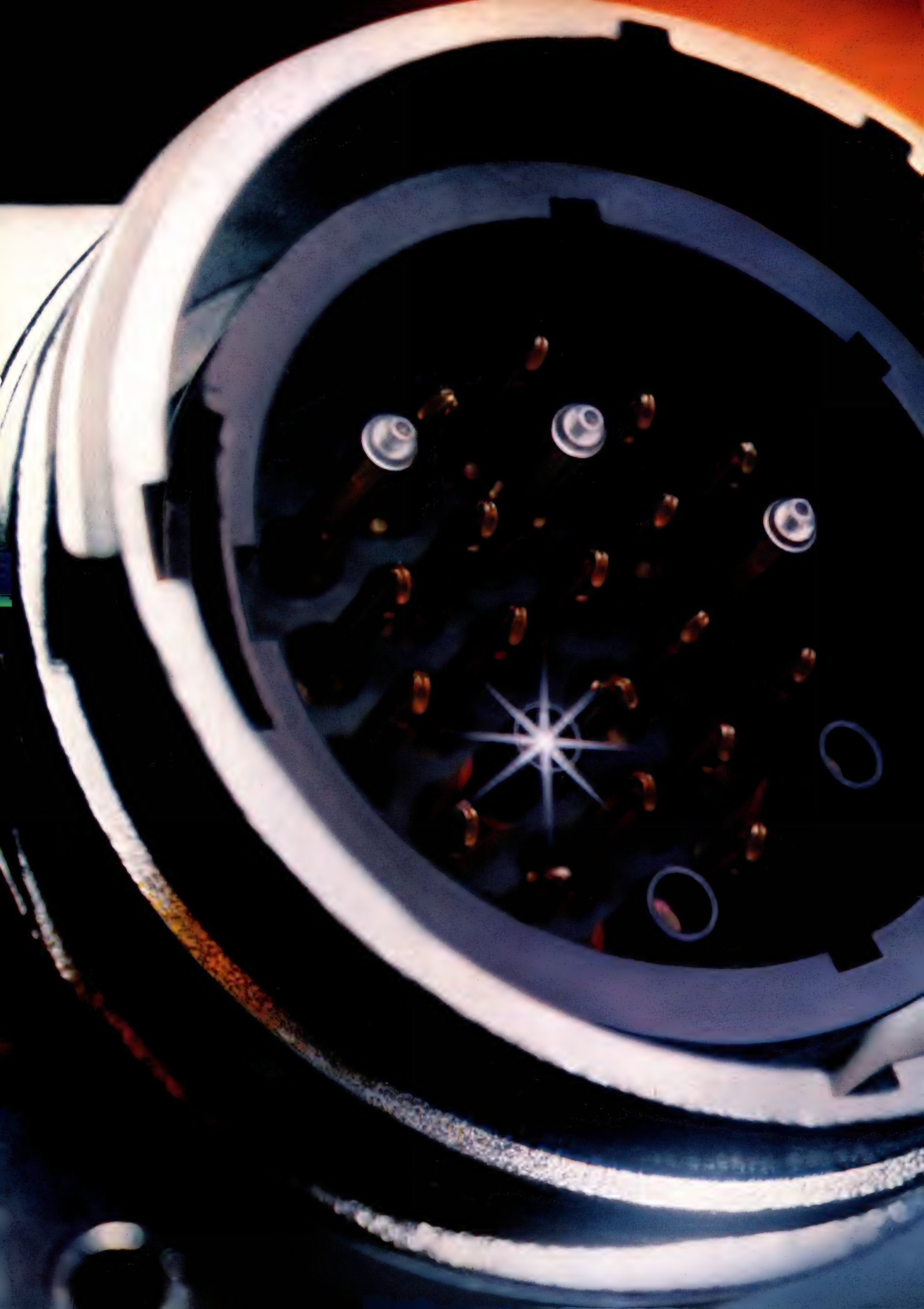

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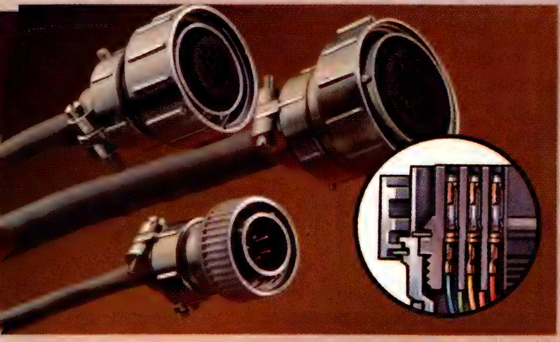

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Simplifying the Tower of Babel

Though decidedly more difficult to get off the ground than word-matching speech recognition, the phoneme-based system favored by Olivetti could offer a host of attractions, once realized. First, because the number of phonemes in a given language is limited, a text containing all of them could be read by a user in a matter of minutes to train the machine for any size of vocabulary. With a word-matching system, the training becomes longer with each word added to the system vocabulary.

Perhaps more important for Olivetti is the flexibility that phonemes offer for dealing with different languages. Even though each language uses different phonemes, the kind of signal processing used for speech recognition remains the same. Word-matching systems have to be constructed practically from scratch for each individual language.

According to Olivetti voice processing manager Vittore Vittorelli, several recognition schemes developed in Japan split the difference between phoneme and word matching; in these approaches, the user speaks in separate syllables, and pattern matching is performed at the syllable level. Such a strategy, he feels, might be acceptable for the Japanese language with its 110 syllables that tend to be spoken separately, but it is not feasible for the connected speech of the Indo-European languages.

In order to adapt its system, Olivetti is doing in-depth research on the five languages in which it is working to define the algorithms that are defined in turn by each language's characteristics. These, along with the phonemes, are the key to speech recognition.

Delineating them for five languages is no mean task. Complicating the issue are differences in the number of vowel sounds (rather than vowels) from a low of 5 for Spanish, to 11 each for English and French. Phonetic-to-alphabetic conversion in Italian, Spanish, and German follows rules to which there are few exceptions; but in English and French it requires complex tables. Once the conversion is made, there is little word-level ambiguity in Italian, Spanish, German, and English. In French, however, it is very frequent—*c'est*, *ces*, and *sais*, for example, all common words, mean very different things but are phonetically nearly identical. **–R. T. G.**

process couldn't be low-profile–emulated." Low-profile emulation is a compromise between total speech recognition and cuing the user for control with sophisticated prompts.

Task divided. Olivetti stresses that this is a research project and that any related product is several years in the future. The company has divided its task into two essential parts: the signal processing necessary to recognize spoken utterances, and the user-machine interface. For the former, work is based on linear predictive coding, principally because it provides both voiced and unvoiced signals, with a pitch value for the voiced signal.

To further aid recognition, the company will also make use of all available information on lexical and syntactic constraints, as well as statistics on the frequency of words and word sequences. Thus, when the voice input is not immediately identifiable on its own merit, the machine might extrapolate the command by using a combination of signal processing and data.

Basically, the incoming voice input will be digitized and sampled at a rate of 18,000 samples per second, or the equivalent of 9 kilohertz, in overlapping windows of 30 milliseconds. The signal is then pattern-matched with the operator's phonemes as defined during a short training period and with the machine's list of acceptable commands. Once identified, it can be treated as any command from any source such as a keyboard.

It is when the machine cannot identify the command—with the data- and signal-processing capabilities at its disposal—that the user-machine interface comes in. According to Vittorelli, the operator must get a real-time feedback as to why the machine does not understand.

"The machine has to tell the operator something like: 'this is what I understand and it isn't a model that I recognize' or 'I can't distinguish between x and y,' so that the operator can correct and, finally, prevent errors," he explains. "What we're really trying to do is to de-emphasize the idea of speech recognition and replace it with the concept of a man driving a machine using speech."

Comparisons. Though too early in the game for the user-machine interface to be defined concretely, Olivetti is experimenting with graphical representations of the operator input that compare this speech signal to, say, the vowel sounds that the machine has extrapolated from the phoneme training session. To be successful here, the company will clearly have to muster all of its expertise in ergonomics.

Though the user-machine interface is sure to evolve, Olivetti is firm in its resolve to stick to phonemic recognition (see "Simplifying the Tower of Babel"). It is convinced its choice offers a richer evolution in dealing with connected speech and avoids the inherent limitations of word-level or template recognition: memory requirements, computation time, and learning time that all grow as the dictionary grows; templates that all have the same weight regardless of their semantic relevance within a given context; and word segmentation in connected speech.

Phonemic recognition, on the other hand, is potentially a far more flexible and user-friendly interface for many reasons, says Vittorelli. It may be speaker-dependent or -independent. Where it is dependent, the learning procedure is limited to a number of phonemes. Also, when recognition is sufficiently precise, word-boundary detection is no longer a problem. Finally, the dictionary structure may include information about the semantic relevance of each phoneme within each of the words used. **–Robert T. Gallagher**

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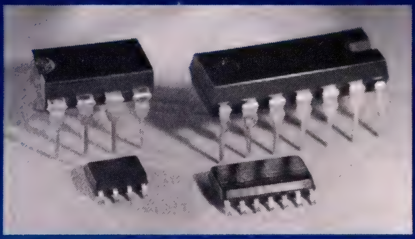

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Circle 193 on reader service card

Entrepreneur Hease launches data base

Since his first job after leaving school—as a reporter on a local East London paper—34-year-old Richard Hease has had several careers: reporter, public relations consultant, technical journalist, and publisher. And true to form, he is breaking new personal ground with his latest undertaking, Micronet 800, a data-base service targeted at the home-computer user.

Micronet 800—a joint venture between Prism Microproducts, East Midlands Allied Press plc, and Prestel, British Telecom's videotex service—will provide hundreds of games, education programs, and other services that personal-computer users can call down directly into their computer over the telephone.

Also available will be electronic mail and message handling, armchair shopping, and news and information about computers, equipment and services. Then, in September, Hease will start Business Micronet, offering business programs plus a connection into the Telex network.

Familiar customer. Hease is addressing much the same user base with his new Micronet Service as he has with a string of computer magazines he formerly published. He launched the first of these—Which Computer—back in 1977 and rapidly followed with a string of highly focused publications such as Practical Computing, IBM User, and DEC User among others. In 1981 he sold all but one of these to East Midlands Allied Press who retained him as a consultant on the magazines and to look over its money-losing two-way videotex activity.

Meanwhile, Hease was busy expanding his own publishing company with a string of new titles such as Sinclair User, Sinclair Projects, and Sinclair Programs. "We want to mop up the personal-computer market," he quips. Hease quickly made a connection: why not use British Telecom's Prestel Viewdata Service to supply news and programs to personal-computer users—a population already numbering over a million in the UK.

Informative. First a reporter and now a data-base marketer, Richard Hease has always been in the information-supply business.

Both Prestel's Richard Hooper and East Midlands Allied Press liked the idea, so Hease set about putting together a launch package. That meant providing sufficient software to interest computer users and also equipping them with a low-cost modem with facilities for downloading software.

Hease's plans now include launching a new modem a month, targeting most popular personal computers. Meanwhile, Micronet is off to a good start, having signed up 1,000 users only one month after opening.

And to confirm that behind every successful person there stands a helpful mate, Hease's wife, a trainee florist when they met, sold some of her florist shops to help get his business off the ground.

Leasametric's Negele profits when Europeans rent

Guido Negele's soft voice and easygoing ways lend him the appearance of a mild-mannered professor or civil servant. But on closer scrutiny, Negele turns out to be a hard-driving executive, one who has built a business from scratch to a multimillion dollar operation in just over a year.

Negele, 42, is head of Leasametric GmbH in Eching, near Munich, West Germany, a company that, like its parent Leasametric Inc. in Foster City, Calif., rents out test and measuring equipment as well as data peripherals and systems. Founded in late 1981, the subsidiary came on the scene when the traditional German bent for ownership was giving way to the more American "why-not-just-rent" attitude.

Anti-investing. Behind the new wave, Negele explains, is the increasing reluctance of the industry to invest in ever more expensive and elaborate equipment for limited use, like microprocessor development systems. "All too often, such equipment is used but once during a project and then never again," he says. "Besides, equipment purchases sometimes entail long delivery times—too long when a test project calls for speedy completion. Renting, on the other hand, means fast availability and spells tax advantages."

Negele's credentials for his position include more than 15 years in instruments. Holder of a master's degree from an engineering school in Munich, he worked for some time as an instrument designer for Rohde & Schwarz in that city, and in 1971 joined Kontron GmbH, also in Eching. There he rose to general manager, a position he still holds.

Speedy reaction to customers' requests for anything from a simple voltmeter to a sophisticated system is Leasametric's forte. Another is the firm's access to its parent's vast stock of items in California—70,000 in all—for anything it does not have on hand in Eching. "Supplying a system—any system—to a customer in Germany generally takes no more than a week, even if it must be shipped from the U. S.," says Negele. Providing documentation and assistance has also helped Leasametric on its road to success.

Rental operations in West Germany, as in most of Europe, are now at a point where they were in the U. S. in the early '70s. "We expect that business to double from year to year at least for the next half decade." To cash in on this trend, Negele has just set up an outlet in Frankfurt and plans to establish two more in Germany—in Stuttgart and Hamburg—before the end of this year. Long-range intentions are to branch out into neighboring Austria, Switzerland, and France. ☐

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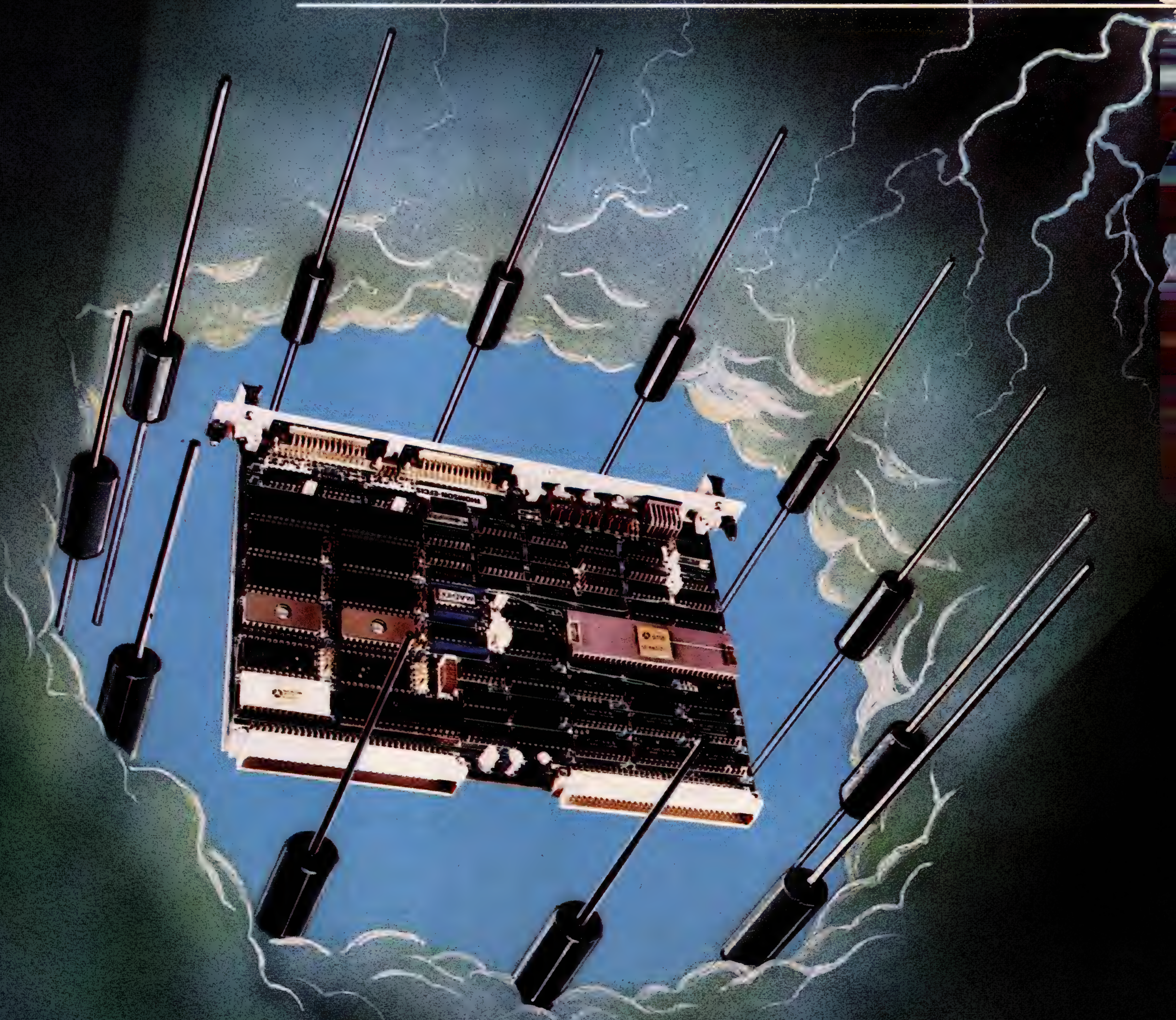

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ue to the great development of ectronics in every kind of industrial fields utomobile, computer, telephony) liability has become an essential oncept.

ficient protection of electronic omponents against short duration vervoltages (that means overvoltages enerally encountered in electronic quipments) allows to increase onsiderably reliability.

RANSIL

ne TRANSIL is a controlled avalanche ode especially designed to clamp vervoltages and dissipate high energy transient operation.

ain characteristics f Transils:

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. **The breakdown voltage or knee oltage V_{BR}** is the voltage value above hich the current in the Transil increases ery fast for a slight increase in voltage.

. **The clamping voltage V_{CL}** as specified the data-sheets is the maximum value r the «standard» pulse with a peak value Ipp, specified for any type of Transil g. 2).

. **Transil's power dissipation** on-repetitive operation). A protecting evice whose operation is adiabatic can dissipate the very same energy.

$$W = \int_0^{\tau} V_{CL}\, i\, dt$$

5. Possibility of power dissipation by Transils in mean power
In repetitive operation, the specification to be considered is mean power P_{AV}.
$P_{AV} = f.W$
(f: frequency, W: energy dissipated at each pulse)

6. Speed
A conventional lightning arrester system only responds with a certain delay which can reach 2 μs. A metal oxide varistor does not respond immediately either (delay of about 25 ns).

If a current with a very low rise time flows through these components, an over-voltage could appear before the device reacts.

In the case of Transils, the avalanche phenomenon of a silicon diode is extremely fast: theoretical value is about one picosecond.

Avantages:

Transils are the only protection components which simultaneously have the following characteristics:

- High operating temperature (175°C maximum),
- Perfect stability of the characteristics in time, i.e. contrary to most other technologies, Transils do not age,
- Extremely short response time,
- Very narrow tolerances on the characteristics,
- Very low dynamic impedance; this leads to a very good clamping factor.
- Transils have high power absorbing characteristics for overvoltages with durations of about 1 millisecond (or more), i.e. overvoltages which are encountered mostly in electronic equipment.

Applications:

Transils can be used as protection devices each time the load will accept neither overloads (limited by V_{CL}) nor a cut in voltage.

ig. 1: main characteristics of a Transil.

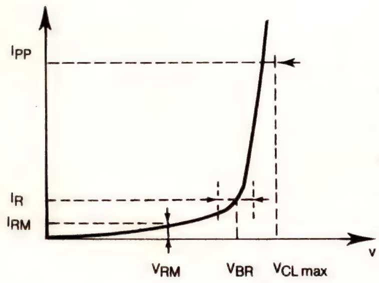
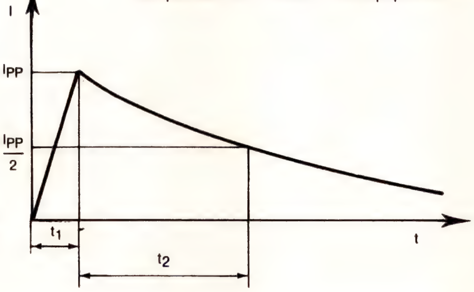


Fig 2: Standard exponentiel pulse. This type of pulse corresponds to most of the standards used for the protection of electronic equipment.



An expanding range

TYPES	P surge (W) 1 ms expo	V_{RM}	CASE
BZW 04 series	400	5V5, 376V	F 126
BZW 06 séries	600	5V5, 376V	F 126
P6KE series	600	5V5, 376V	CB417
BZW 11 series	1000	10V, 110V	DO 27A
1N 5629 1N 5665A	1500	5V5, 171V	DO 13
1N 6036 1N 6072A	1500	5V5, 185V	DO 13
PFZ series DTZ series	1500	5V5, 376V	DO 27A
BZW 25 series	2500	12V, 120V	DO220AB
GLT series	2500	12V, 120V	DO 4
BZW 30 series	3000	12V1,486V	DO 27 A
BZW 50 series	5000	8V2, 180V	AG

and for the protection of microprocessors, integrated circuits, C.MOS and MOS:

T. GMP 5 series	600	5V	F126
1N 5907	1500	5V	DO 13
1N 5908	1500	5V	DO 27A
T. ICTE 5 series	1500	5V → 45V	DO 27A

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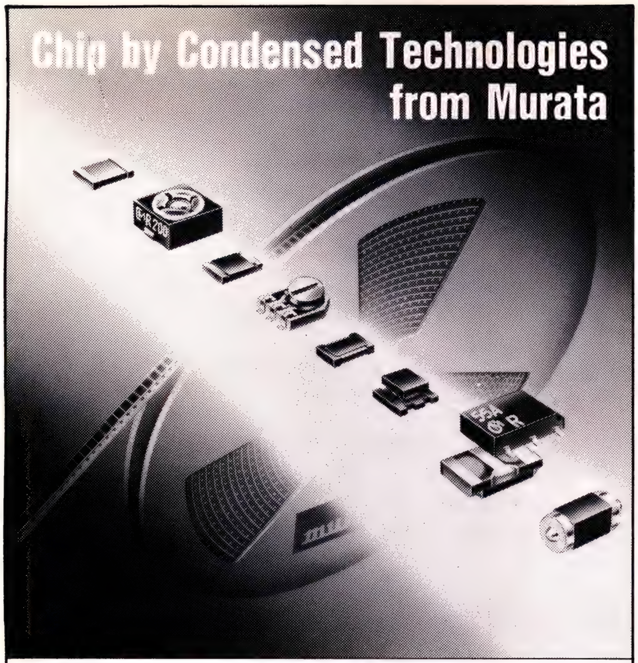
DIVISION SEMICONDUCTEURS

OU MAY DEPEND ON US, WE'RE NEVER FAR-AWAY...

Circle 194 on reader service card



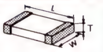
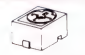
Murata leads the chip age with its technology, leaving others far behind.

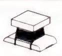
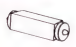
Electronic chip components are largely changing mounting concepts for all electronic apparatus.

Murata inaugurated the development of chip components first and foremost by anticipating the needs of the times.

Including the monolithic chip ceramic capacitor, Murata suceeded in developing 9 kinds of chip components; chip coil, variable chip resistor, chip trimmer, ceramic filter and ceramic resonator.

Murata, a pioneer of the chip age, aims to make all its components into chips.

MONOLITHIC CHIP CAPACITOR	CHIP TRIMMER CAPACITOR	CHIP RESISTOR	CHIP SEMI-VARIABLE RESISTOR	
		RX29/39		
				
3.2×1.6×0.7 2.0×1.25×0.7	4.5×4.0×3.0	3.2×1.6×0.57 2.0×1.25×0.47	4.5×3.8×2.3	

CHIP CR NETWORK	CHIP COIL		CHIP FILTER		CHIP RESONATOR (Ceralock®)
	LQN5N	LQN3N	AM	FM	
					
3.2×1.6×0.7	5.0×4.0×3.15	3.2×2.5×2.0	7.0×4.5×2.1	6.3×3.9×1.5	6.8×2.8×2.6

SIZE:L×W×T(Unit:mm)

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Circle 195 on reader service card

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New products international

Slow-scan TV unit uses phone lines, can detect motion

by Robert Gallagher, Paris bureau manager

Microprocessor-based system sends image every 1.1 to 6.5 s, can be programmed to sound alarm when picture changes

Useful as closed-circuit television might be for certain communications and surveillance applications, the coaxial cable or radio link made necessary by the high bandwidth of the signal transmitted from camera to monitor can often make it an uneconomical proposition. One way around this limitation for a wide variety of applications is slow-scan television that uses standard telephone channels as a transmission medium.

Such a system has been developed by the Societá di Elettronica per l'Automazione SpA, a Turin-based subsidiary of the Fiat group. The microprocessor-controlled system can process pictures in a variety of ways and is useful as an automatic detection system for centralized surveillance applications.

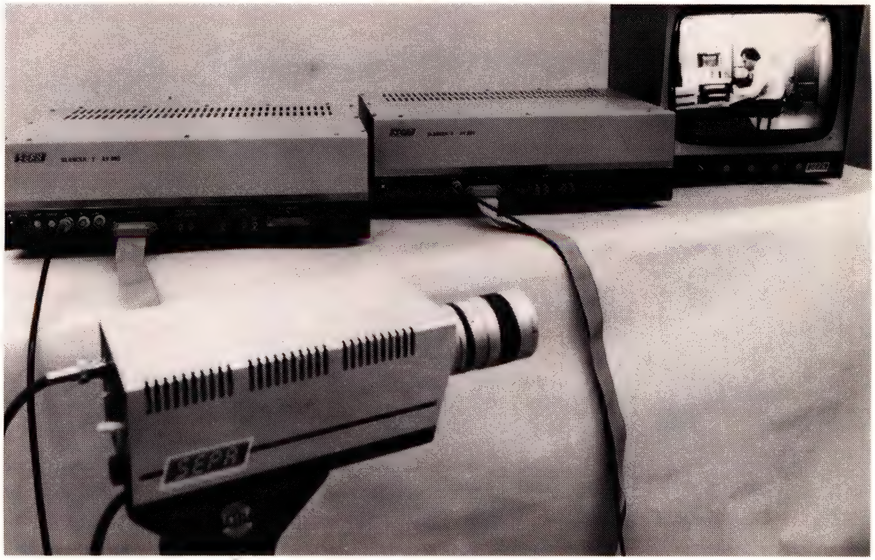
The transmission medium of a television system cannot be downgraded without sacrifice, and in the case of SEPA's system, the loss is in image continuity—the system transmits a series of still pictures at fixed intervals. Nonetheless, in addition to security, the Still Picture Television System is useful for remote conferencing and instruction where drawings, text, slides, and so on, must be transmitted. It can be used to send X rays, ultrasound pictures, and nuclear scans for remote medical applications. The completely digital system can also serve as interface between TV camera and computer.

The basic system consists of a transmitting unit and a receiving unit, each with a modem. From the output signal of a standard European black and white TV camera, one frame is sampled and stored in a random-access memory during a period whose length depends on resolution and transmission mode. The system's Z80-based central processing unit reads the data and sends it in a serial stream to the modem, which transmits it on a telephone channel.

In standard operation, each of the 256 lines that make up an image consists of 256 picture elements, each coded as 6 bits, corresponding to 57 gray levels. But by choosing between different resolution formats (256 by 256, 128 by 256, 256 by 128, and 128 by 128) and between 6-bit pulse-code–modulation transmission and 4-bit differential PCM, it is possible to trade off image quality with updating speed. Using PCM in maximum resolution, one frame is sent every 6.5 s; with minimum resolution and differential PCM that time drops to 1.1 s at a transmission rate of 64 kb/s.

When employed for centralized surveillance, the user can take advantage of the way pictures are stored in consecutive frames. Based on the standard transmitting and receiving units, it requires additional software, as well as an operator's panel and a signal panel, and can monitor up to eight different areas at a time.

Motion alarm. The camera of each transmitting unit is aimed at a surveillance target where one would normally expect no movement, like a fire escape or private courtyard. Transmitting at a rate of 4.8 kb/s, it sends only those pixels that have changed from the last frame to refresh the image. The transmitting unit, equipped with a software-based motion detector, generates an alarm when the picture alteration exceeds a preset threshold. When the alarm sounds, the camera zooms in on the



location where change has occurred.

SEPA's first customers will be the Italian police, who plan to use the system for traffic surveillance. The country's postal service intends to install a teleconferencing facility between Turin and Rome. Commercial production is planned for the end of this year, with a color coaxial-cable version available for 1984. Price depends on the configuration chosen.

Societá di Elettronica per l'Automazione SpA, Corso Giulio Cesare 294, 10154 Torino, Italy [441]

Modular system for data acquisition and control plugs into Multibus cage

British start-up Di-An Micro Systems Ltd. has an attractively simple approach to setting up Multibus-based measurement and control systems. The user configures the board to his requirements by plugging in the appropriate modules selected from a library of analog and digital input/output and converter modules.

Any 8- or 16-bit Intel iSBC or Multibus-compatible computer can then be used to control test and measurement rigs. A single DMS531 board will support up to 64 analog input channels, 16 analog output channels, or 64 digital I/O lines in various combinations.

Larger systems can be assembled by adding more boards. In such multiple-board configurations, each I/O channel maps directly into the controlling microprocessor's memory, with each board having a different base address. The DMS531 supports 20-bit addressing and appears as 32 consecutive memory locations.

On a DMS531 board measuring 12 by 6.75 in., there are sockets for four I/O modules plus a fifth dedicated socket for an analog-to-digital converter module. Selected modules connect directly into an internal component-level bus called Columbus. The rest of the card comprises a bus-interface chip plus interrupt-control logic that interfaces the Columbus to the Multibus, an optional dc-dc converter module, plus a choice of analog converters.

All the I/O modules in the interface library have been squeezed into a standard size by the use of miniature components on a small printed-circuit board. Interface cards targeted at buses other than the Multibus require only the developement of a motherboard into which the standard modules can be plugged.

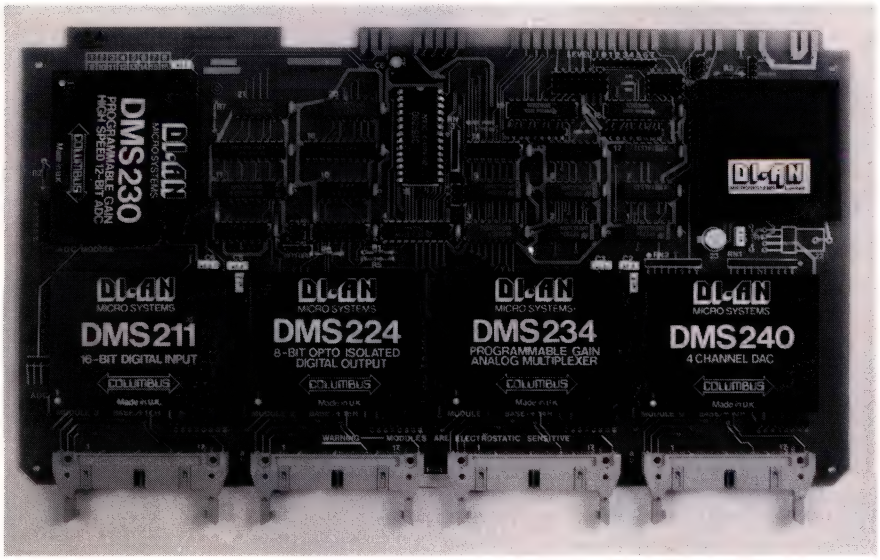
For example, the company has already produced an interface card, the DMS550, for the IEEE-488 bus. It is targeted at users of the Apple, Commodore, and Hewlett-Packard personal computers. It also plans a VME board soon. By creating a common I/O structure in this way, says Geoff Redman, Di-An's sales and marketing director, the company can achieve production and development economies. That way, he believes, the relatively small firm can compete head on with bigger outfits like Adac, Analog Devices, Burr-Brown, and Data Translation.

The analog input modules have 8 differential or 16 single-ended inputs. They feature software programmable gain, automatic zeroing circuitry, and internal calibration facilities.

Conversion tradeoff. A-d converter modules can be chosen for noise rejection or speed. The DMS231 integrating analog converter module has a high common-mode rejection ratio of 130 dB and a resolution of 13 bits plus sign. The DMS230 high-speed converter offers throughput rates of 100 kHz and 12-bit resolution. Conversion can be either under program control or by means of an external trigger. Programmable gain in the DMS234 multiplexer module permits low-level analog input capability down to +5 mV full scale.

Digital input modules accept active signals over a wide voltage range or sense contact closures. They offer input filtering and 500-V optical isolation as options. Digital output modules are designed to drive industrial loads such as relays and lamps, the range including the DMS224 optically isolated unit, which is capable of switching 80-V, 1-A loads.

The DMS531 supports both polled and vectored interrupts, and uses a flexible software-configurable interrupt-control method in which interrupt vectors are selected and configured through the bottom two address bytes. A program may modify the vector address to suit the interrupt service required to satisfy a particular module, rather than relying on the usual technique, in which interrupts always vector to the same location, and then require computation of the action to be taken. The user may choose one vector for each I/O module or one vector for several modules. A jumper determines the



SIEMENS

The Energy-Saving Computer

Heating costs are high. So far, analog heating control systems reacting to outside temperature changes, have been used to save energy. But only the microcomputer has answered the call for greater economy and simplified construction together with high performance capability. It therefore permits significant improvements in such heating control systems.

A new development from Siemens – the single-chip microcomputer SAB 80215 – with its integrated, application-oriented peripheral features provides the performance demanded:
- highly sensitive control system
- maximum operating convenience
- temperature control individually programmable for every day of the week
- timer
- protection of timer and all input data in case of power failure
- measurement and display of different temperatures
- sensor monitoring for line breaks or short circuits
- alarm signal in case of incorrect operation.

The Siemens single-chip microcomputer SAB 80215 is equipped with the extended 8021 processor (2-Kbyte ROM, 128-byte RAM) and integrated peripheral units, such as:
- A/D converter and counter
- clock with stop function and alarm call
- keyboard inquiry, display control and
- closed-circuit operation.

This makes a lot of other applications possible. For further details simply write to Siemens AG, Infoservice/B 8304-101, Postfach 156, D-8510 Fürth, quoting "SAB 80215".

Single-chip microcomputer SAB 80215 from Siemens

B 8304.101

Circle 196 on reader service card

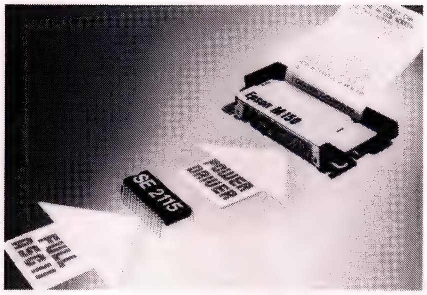
interrupt-request line that is used.

The DMS531 draws its power from the Multibus +5-V line, and an on-board dc-dc converter provides ±15 V to drive the analog I/O modules. For applications requiring the use of digital I/O modules only, the DMS531 is available without the dc-dc converter.

Di-An Micro Systems Ltd., Mersey House,
Battersea Road, Heaton Mersey, Stockport,
Cheshire SK4 3EA, England [442]

Single-chip driver serves GMT system 700 series printers

The SE 2115 single-chip printer controller can be used in the GMT system 700 series printers, which have Epson M-150 and M-160 dot-matrix mechanisms and an interface board with all the circuitry necessary to operate a printer working from parallel or RS-232-C type ASCII signals.



Operating from a single 4.5-to-6-V supply, the SE 2115 has a 96-character ASCII set that includes the £ sign and generates true descenders. In addition, inverted print is possible, and dot-addressable graphics can be generated on a field 96 or 144 dots wide, depending on the printer mechanism. Also, a self-checking facility tests the operation of the chip and the printer mechanism.

The SE 2115 is priced at £13 in single units. In lots of 100, it will cost £9.75.

GMT Electronic Systems Ltd., Newport
House, 22 Hartfield Rd., Wimbledon SW19
3TD, England [444]

Terminal is compatible with HP and DEC stations

Combining DEC VT100 and Hewlett-Packard block-mode capability, the 828 terminal is ideal for multisystem sites. For only £1,996, the unit does the work of a VT100 plus an HP mode terminal all in one unit, whereas a VT100 plus an HP block-mode terminal would normally cost in the neighborhood of £3,000.

With the 828, operators need only learn how to use one terminal and one keyboard. Simply flipping a switch changes the 828 from one type to the other.

The terminal has as standard a 32-K-byte memory, full editing capability, a buffered printer port, high-resolution 80- or 132-column display, host-loadable fonts, and a fold-up detachable keyboard. In addition, the 828 can be used with any system supporting glass teletype or ANSI-

standard computer terminals.

Direct Ltd., 12 Rufford Court, Hardwick Grange, Woolston, Warrington WA1 4RF, England [445]

Unit can program E-PROMs 16-K to 128-K in size

In the offing from Mercury Systems Inc. is a portable programmer for erasable programmable read-only memories that can handle a wide range of E-PROMs from 16- to 128-K in size, such as Intel's 2716, 2732, 2732A, 2764, 27128, 2815, and 2816; Texas Instrument's TMS2532 and TMS2564; Motorola's MCM68764; Hitachi's HN48016; Mostek's MK-2764; and Fujitsu's MBM2716, 2732, 2732A, 2764, and 27128.

With Super-EX model SE4941, the Fujitsu MBM2764 and the Intel 2764 and 27128 can be programmed in only one quarter to one eighth the time taken by the conventional algorithm. Its functions include blank check, programming, read check, copy read check, and erase blank check. Data-editing functions include 1-byte acknowledge and updating, data complement, insertion, deletion, block storage, block moving, data searching, splitting, and shuffling.

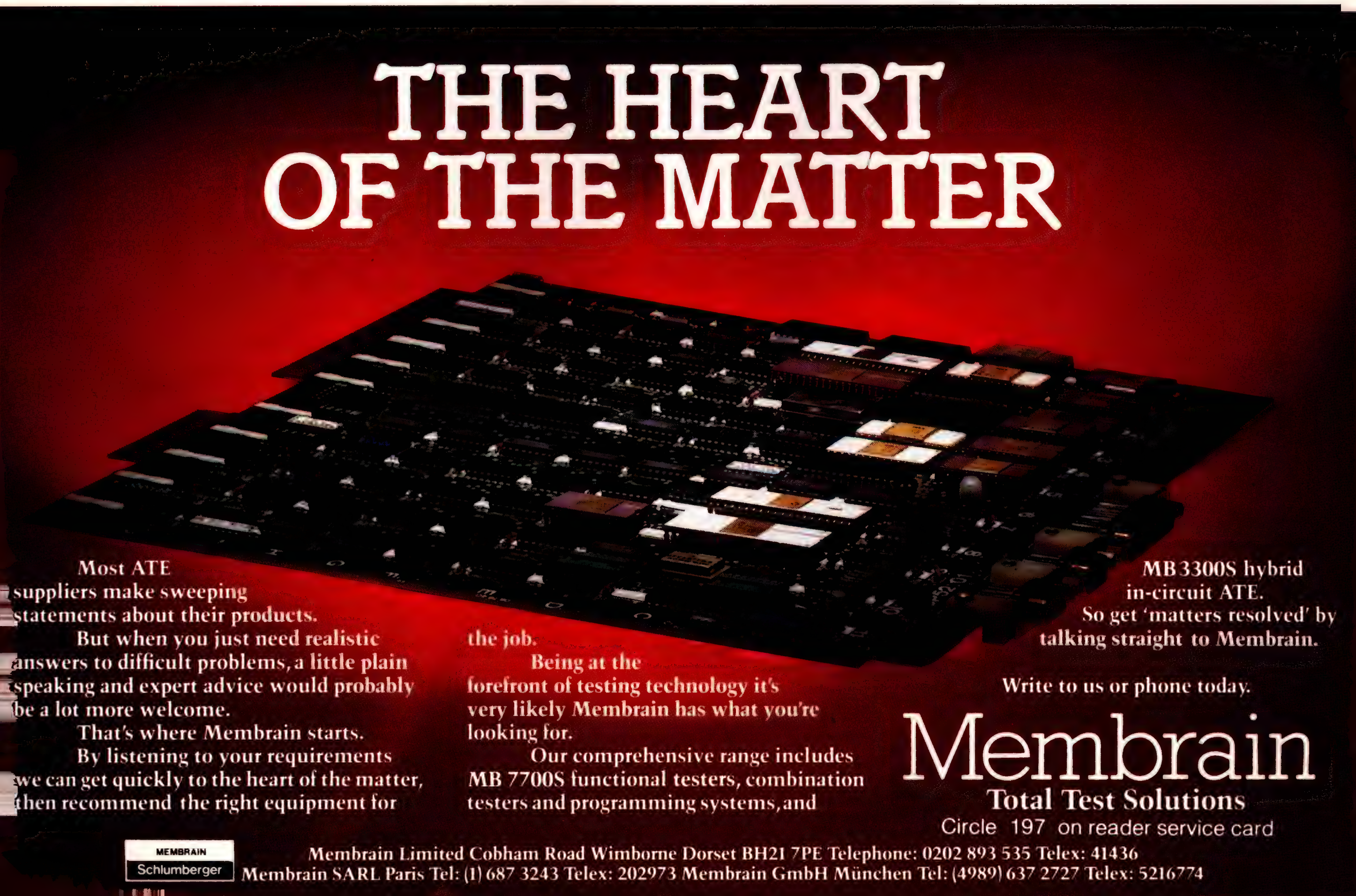
The model SE4941 accommodates binary, ASCII hexadecimal, Intellec Hex, Motorola EXORmacs, and Tektronix standard and extended hexadecimal transfers. It has reliability checking and protection features and self-diagnostic fur memory, display, age, and timing c interface that r rates of 100, 300, 600, 1,200, 2,400, and 4,800 b/s is standard. The programmer requires 85 to 249 V ac input at 50 to 400 Hz. Power consumption is approximately 17 VA.

The SE4941 Super-EX E-PROM programmer is $1,500 in the U. S.

Mercury Systems Inc., C. P. O. Box 1974, Tokyo 100-91, Japan [447]

Automatic inspection tool serves industrial applications

Designed as a powerful automatic inspection tool for applications such as robot vision, biological-image analysis, quality control, noise reduction in low-light situations, spatial measurements, object tracking, optical character recognition, and other industrial uses, the CRS 1000 is based



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ROVIDING A SCIENTIFIC EY

Take a good look at the photograph below. Is it a gas nebula somewhere in the universe or a microcosm here on earth? Astronomy, metal physics, or human biology? Such are these scientific disciplines that if the yardstick by which they were measured were distance, they would literally lie worlds apart. Astronomy is the study of all objects within the universe; metal physics the properties governing solid state materials and biology the phenomena of life. Despite the divergent nature of these sciences, their individual development can be traced back to a single unifying source: the Galilean telescope invented in the early 17th century to examine the stars and planets. That same telescope, modified and viewed through the other end, became the microscope - the key to the exploration of inner space. In the course of the last three centuries parallel development of optical telescopy and optical microscopy has provided scientists with deeper and deeper insight into hitherto invisible worlds. However, the application of electronic and computer technologies as tools for scientific investigation has achieved a much greater impact in considerably less time.

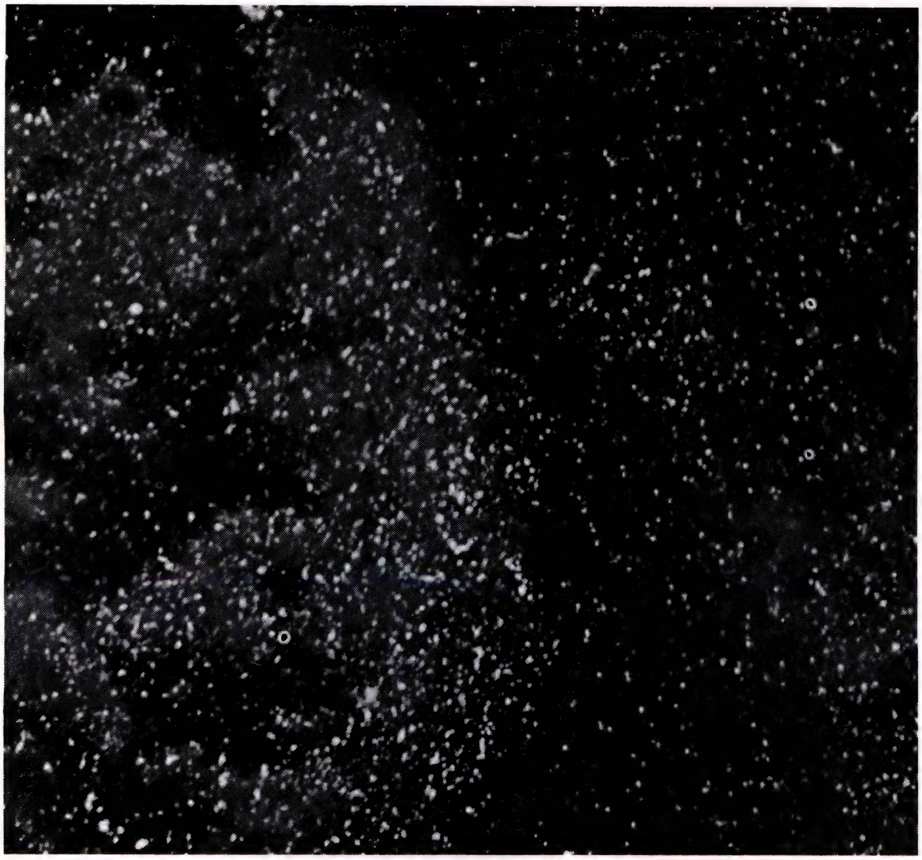
The electromagnetic spectrum, like the optical properties of Galileo's telescope, has provided a fundamental basis for development of a wide and varied range of sophisticated investigative instrumentation over the past three decades. Astronomy, metal physics and biology have benefited, of course. But the interdisciplinary nature of this development has given impetus to other fields of research such as Chemistry, Radiology, Geology, Meteorology, Telecommunications and Microelectronics.

As one of the world's leading research-based electronic enterprises, Philips has played an important role in this technological evolution. Notable achievements in electron microscopy start with selected-area diffraction apperturing and a 5-lens optical system in 1949, and continue with similarly innovative 'firsts' through to the recent introduction of a new family of transmission electron microscopes. Indeed, Philips global reputation for innovation in this field applies not only to electron optics, engineering and vacuum design but also to their application-oriented system concepts.

For medical investigations, Philips has developed advanced diagnostic systems for CT scanning, digital vascular imaging (DVI), ultrasonics and nuclear magnetic resonance (NMR). And you will find Philips providing a scientific eye for detail in space technology, too. In radio telescopes, in satellite earth stations and on board orbiting astronomical satellites.

For a closer examination, here are some fine details.

Circle 224 on reader service card



Outer space or inner space? Inner space, in fact. The bright spots represent the distribution of minute palladium catalyst particles 0.000004 mm in diameter on a thin substrate. The image was recorded using the conical dark field mode of the Philips EM 400T transmission electron microscope.

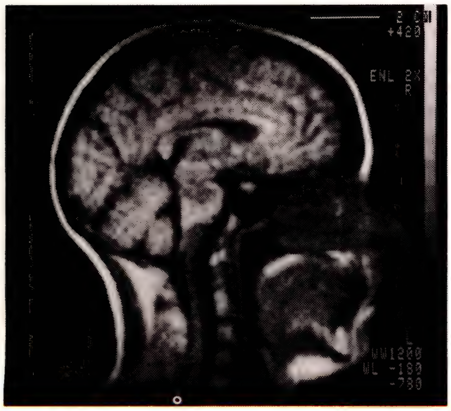
PHILIPS

FOR DETAIL

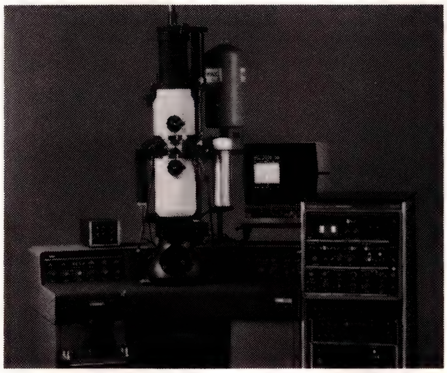
NEW NMR SYSTEM FOR MILAN CLINIC

Measurement of the nuclear magnetic resonance (NMR) of hydrogen is a long established analytical procedure in chemistry and physics. Now Philips has applied this principle to develop the GYROSCAN - a NMR medical diagnostic system for visualizing internal organs and other tissues. NMR makes use of the property that hydrogen nuclei, which are present in all living tissue, can be made to emit radio signals. Using computer techniques, these signals can be processed to obtain an image of the tissue-of-interest. Good results have been achieved in the detection of brain oedema and the study of pathological processes such as necrosis, ischaemia and various types of neoplasm and degenerative disease.

The GYROSCAN has been ordered for the Radiology department of the Clinic Pio X in Milan, Italy, where a Philips TOMOSCAN 300 CT scanner has already been used for over 30,000 studies.



Circle 225



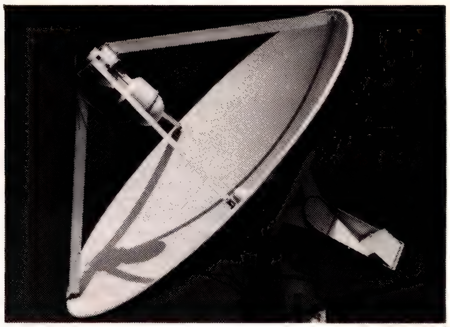
NEW TEM FOR APPLIED RESEARCH

Philips universal transmission electron microscope, the EM 420, combines high performance imaging with extensive analytical systems capability. A unique feature of the patented Twin lens is that the excellent objective lens coefficients in TEM and STEM are identical and also allow small-probe TEM performance with high ±60° tilt and high resolution. The EM 420 can be extended with an extensive array of accessories to meet advanced specialistic needs in the area of X-ray, electron energy-loss and diffraction analysis. Specially developed for applied research, the EM 420 is part of a new family of transmission microscopes, the others being the EM 410 for life science investigations and the 300 kV EM 430 microscope for fundamental research.

Circle 226

NEW GROUND STATION FOR METEOROLOGY

Signaal, Philips space-tech company, has developed a meteorological ground station that produces instantaneous images from orbiting and geo-stationary weather satellites. Employing sophisticated computer-tracking techniques, the station tracks low-orbiting satellites when they are in range and - when they go out of range - switches over to geo-stationary satellites. This dual-tracking capability enables meteorological agencies to widen their data base by comparing the high-resolution/limited area data from the TIROS-N satellite with synoptic data from the GOES and GMS satellites. The station's software-oriented layout permits a variety of system configurations to be achieved. One of these stations is already operational at the Royal Netherlands Meteorological Institute, KNMI.



Circle 198

These are just a few examples of Philips advanced technology. If you would like more information, contact your Philips organization or Philips Corporate Planning and Marketing Support , VOA-0217, 5600 MD Eindhoven, the Netherlands. Telex: 35000 PHTC NL. Please indicate in which of the above subjects you are interested:

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358

PHILIPS

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on the Motorola 68000 processor, whose 32-bit architecture and instruction set allows complex processes to be performed efficiently.

The CRS 1000 has a large direct-addressing range, which makes it particularly suited to image processing applications. Up to sixteen 512-by-512-pixel images can be accessed directly by the processor at speeds of up to 25 frames/s. In addition, the system uses 6- or 8-bit video analog-to-digital conversion modules permitting full-range gray-level images to be acquired.

The CRS 1000 utilizes plug-in special-purpose hardware modules that perform specific tasks such as convolutional filtering, edge detection, and averaging at speeds far in excess of any processor-based system. For applications that require high resolution or precise measurement, the system may be used with a solid state CCD line-scan sensor.

Computer Recognition Systems Ltd., Unit 5, Fishponds Road, Wokingham, Berks. RG11 2QJ, England [448]

Graphics terminal is aimed at OEM and volume end users

Sporting a price of $2,600, the NJC-M1212 graphics display terminal is suitable for business graphics, graphics information retrieval, and some computer-aided design and manufacturing applications.

The terminal comes in a compact package that contains a high-resolution monitor, graphics processor, communications package, and keyboard. It includes a 12-in.-diagonal high-resolution green cathode-ray tube with 640-by-486-dot resolution, 1-μs/dot high-speed drawing, three communications ports, a Tektronix 4010/4014 emulator, and an optional DEC VT100 emulator.

Designed with the original-equipment manufacturer and volume user in mind, the NJC-M1212 can be specified for delivery in a wide variety of configurations.

Nippon Computer Co., Naito Building, Nihonbashi Hamacho 2-25-1, Chuo-ku, Tokyo 103, Japan [449]

Standard cells hatch semicustom micros

Aiming single-chip systems at high-volume consumer markets, partisans of cell-based design rally at Custom IC Conference

by Roderic Beresford, Solid State Editor

No longer limited to command performances at the large, wealthy system houses, custom and semicustom integrated circuits are dressing up for a starring role in all but the smallest firms' product plans. Among the diverse participants at the Custom Integrated Circuits Conference, May 23–25 in Rochester, N. Y., a few small, fast-moving companies are beating a path to single-chip systems for the consumer markets.

As they open up cell-based design methods to chip users, firms such as VLSI Technology Inc. in San Jose, Calif., and Zymos Corp. in nearby Sunnyvale are adding stripped-down microprocessor "cores" to their repertoires, anticipating a next generation of large-scale ICs that will replace single-board 8-bit systems.

Even now, 4-bit cores for customized microcontrollers, such as those from Integrated Circuit Systems Inc. of King of Prussia, Pa., are aiming at the juicy target formed by standard chips like those of Texas Instruments Inc. of Dallas. TI, meanwhile, is cultivating more computationally intensive applications with rapid additions to its 8-bit line.

The unquestioned economies of higher integration justify the working assumption of the entrepreneurs that the end goal in most applications is a single-chip system. "Today we are on the verge of being able to put complete 8-bit systems on a chip," says Wes Patterson, director of VLSI systems at VLSI Technology, a supplier of design technology and foundry services.

"At that level of integration—the complexity of today's home and video-game computers—the chip is replacing a printed-circuit board," he adds. His company concludes that system designers must get involved at the chip level and that conventional semicustom techniques like gate arrays and standard cells will not carry the day.

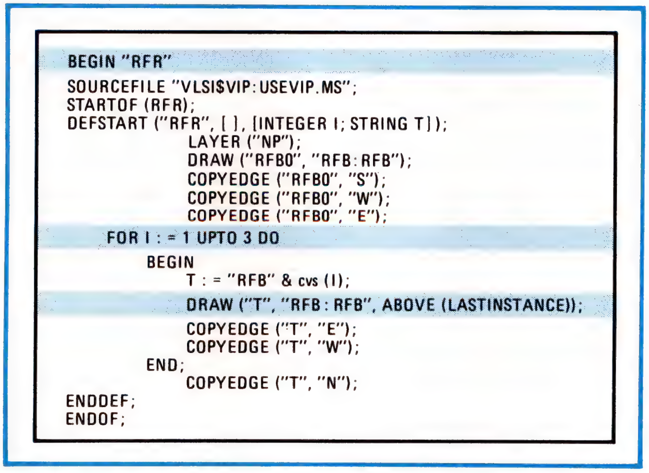
Rather, those VLSI systems will comprise two levels of building blocks. "One level is going to be fixed and standard: the core of a microprocessor like the 6502, Z80, or whatever," continues Patterson. As will be discussed at the conference, VLSI Technology's second level is a set of cell compilers for all the components that go along with such a standard core: input/output structures, counters, timers, and random-access and read-only memory. The compilers are programs (written in Mainsail, a compiler language developed at Stanford University, Palo Alto, Calif., and marketed by Xidak Inc. in neighboring Menlo Park) that draw detailed mask geometry from a handful of parameters entered by the user (see below).

Earlier this month, VLSI Technology was completing negotiations with a microprocessor supplier to license a popular 8-bit design for just such uses as a core in custom systems. Other, more fundamental problems also face these would-be architects of single-chip machines. "Embedding a microprocessor in a bunch of other system logic presents a huge testability problem," notes Patterson.

Chip squeeze. Chip size is another obstacle because the present capabilities of the semicustom industry mostly fall in the range of 3-to-5-micrometer geometries. "Even if you have the mask data for a 6502, for example, which takes up only about a quarter of a 220-mil chip, you still have to fit everything else in without wasting a lot of area.

"Beyond around 250 mils, you may be better off with two chips. In other words, memory will be the last component brought on board," concludes Patterson. Finally, practical packaging options limit power dissipation to 1 to 1.3 watts. H-MOS (high-performance MOS) designs quickly run over that power budget; therefore, VLSI Technology is eagerly gearing up for a complementary-MOS capability, of the kind competitor Zymos Corp. already has in place.

"In the next wave of processing-technology improvements—down to



```
BEGIN "RFR"
SOURCEFILE "VLSI$VIP:USEVIP.MS";
STARTOF (RFR);
DEFSTART ("RFR", [ ], [INTEGER I; STRING T]);
                  LAYER ("NP");
                  DRAW ("RFB0", "RFB:RFB");
                  COPYEDGE ("RFB0", "S");
                  COPYEDGE ("RFB0", "W");
                  COPYEDGE ("RFB0", "E");
      FOR I := 1 UPTO 3 DO
            BEGIN
                  T := "RFB" & cvs (I);
                  DRAW ("T", "RFB:RFB", ABOVE (LASTINSTANCE));
                  COPYEDGE ("T", "E");
                  COPYEDGE ("T", "W");
            END;
                  COPYEDGE ("T", "N");
ENDDEF;
ENDOF;
```

Compiling. Mainsail program generates layout for register file RFR in VLSI Technology's system. DRAW repeats register bit RFB.

1.5-μm geometries—we're definitely going to see single-chip 8-bit systems," agrees Bill Loesch, marketing manager for Zymos, the Sunnyvale, Calif., supplier of standard cells. However, he adds that "the market you can point to today is for 4-bit machines" as microcontrollers in appliances and other consumer goods.

Less is more. Although small computers are a big market and growing fast, 4-bit microcontrollers sell in phenomenal quantities. The most popular 4-bit machine—TI's TMS 1000 series—has passed the 60 million mark in cumulative volume.

Zymos's 4-bit core microprocessor, trademarked ZyCOMP 4, was a tough compromise for Loesch. "Not having a standard architecture has been a drawback," he says. "People ask for machines they know, software and instruction sets that are familiar. We looked at both TI's TMS 1000 and National's COPS family, but their instruction sets are too limited. So we designed a 4-bit machine with an instruction set resembling an 8-bit one—Intel's 8049."

Assembling. Zymos's approach to semicustom microcontrollers uses predefined or preassembled standard-cell clusters.

Intel Corp. has not ignored the compliment—or the threat—that semicustom-chip suppliers present to the market for standard microcomputers. A recently signed agreement commits the Santa Clara, Calif., chip maker to supplying at least three designs to Zymos for inclusion in its 3-μm C-MOS cell library.

One will in fact be a core of the 80C49, a C-MOS version of the 8-bit microcomputer, that Loesch says will be available by the fourth quarter of this year. Another will be a universal asynchronous receiver-transmitter cell; eventually, envisions Zymos, a variety of such peripheral chips will be available as options accompanying the core.

Meanwhile, the company has completed the pieces for single-chip 4-bit systems. At the conference, senior engineer Dick Fillmore will report on the RAM and ROM blocks. Fillmore has created "column slices" 32, 64, and 128 words deep to handle any word width.

Cell libraries themselves are nothing new for chip makers. Nor are microprocessors anything new for users. "What is new," concludes Loesch, "is the idea of routinely adding programmability to a user-designed circuit."

David amid Goliaths. Therefore, competition for Zymos and VLSI Technology comes not just from suppliers of standard microcomputer families like TI but also from the likes of Integrated Circuit Systems, a $2 million custom-IC maker. Its cell-based 4-bit n-channel MOS microprocessor has been tailored to the varied requirements of giant-volume users. At the conference, president Ed Arnold and colleagues will discuss their 4-bit core, which they integrate with as much of a customer's system as possible.

"It's our opinion that almost all the control functions in a typical application can be accomplished in 4-bit machines," Arnold says. Rather than gearing up for 8- or 16-bit core processors, the company feels pressure to implement the 4-bit core in C-MOS. "The push from industry is to low power for battery-operated products," he adds.

"Moreover, it's not yet possible to implement an 8-bit system on a single chip," notes Arnold. "TI's TMS 7000 is one approach, but it's a multichip setup. In a 4-bit machine, it's easy to optimize an instruction set around particular functional requirements—say, 50 or 60 instructions. But with an 8-bit processor, the instruction decoder becomes complex."

More or less agreeing, officials at TI's Programmable Products division in Houston say the TMS 7000 is following much the same path as the 4-bit TMS 1000 family, serving specific market sectors with tailored I/O interfaces. "At this point, the place where we see most of the action in the semicustom arena is at the low end—the consumer, automotive, and telecom segments," says Gerald Rogers, division manager.

16-bit talk. "In most of the 16-bit applications now, people are talking about host CPUs, large address spaces, and things like that," he states. "In the consumer, telecom, and byte-oriented computer-peripherals areas, you want to do a lot of bit manipulation, a lot of I/O manipulation, status, control, flags, and so on."

Rogers estimates it will be a couple of years before the 16-bit market will be at the same stage of "semicustomization" as the 8-bit arena. So TI is adopting a wait-and-see attitude toward its agreement with American Microsystems Inc. of Santa Clara, Calif., which plans to market Alterable Microcomputer Units based on the 99000 processor [*Electronics,* Sept. 22, 1982, p. 151].

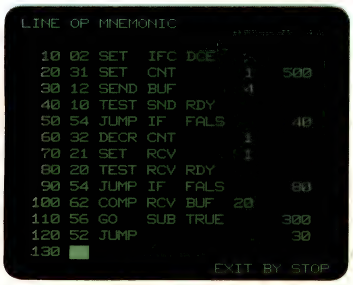
If market acceptance and demand materialize, TI will consider that approach at the 16-bit level. But for now, says business development manager Jim Huffhines, the company's 7000 series serves much the same segments as the units will address.

On the other hand, AMI sees the units and other standard macros—clusters of standard cells—pulling customers away from standard microcomputer chips as well as from fully custom implementations. William Van Zanten, vice president for marketing at AMI, continues to consider lower-end markets such as those the 4-bit cores are attacking. Still, he says the company is more comfortable with its position at the "top of the triangle": selling smaller numbers of more complex chips at higher average prices. ☐

Additional reporting: Marilyn A. Harris, J. Robert Lineback

Don't vacillate
se DA-10 data simulation and test programs

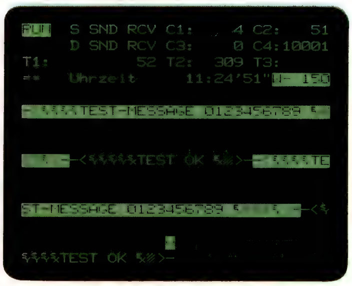
itical attitude towards data s and systems will give security prevents crashes. The DA-10 its simulation mode offers the balance: picking the right ocol is now a breeze. Simple gramming, a multitude of cro commands supported by werful compiler, a total of ommands to send, receive, pare data, with loops, jumps, outines, and the possibility to and reset the interface leads, nake your life easier. Measure time intervals, count events, track of time-outs and get nt-out of the accumulated lts. The universal command kage even permits alteration of fixed procedures. The DA-10 will generate data sequences for almost all common asynchronous and synchronous HDLC protocols (e.g. BSC, MSV, SNA, X.25, Teletex, Btx). In an emergency one simply calls up the right program from the built-in cassette recorder.



```
LINE OP MNEMONIC

  10 02 SET  IFC DCE
  20 31 SET  CNT         1     500
  30 12 SEND BUF         4
  40 10 TEST SND RDY
  50 54 JUMP IF  FALS           40
  60 32 DECR CNT         1
  70 21 SET  RCV         1
  80 20 TEST RCV RDY
  90 54 JUMP IF  FALS           80
 100 62 COMP RCV BUF  20
 110 56 GO   SUB TRUE          300
 120 52 JUMP                    30
 130 █
                         EXIT BY STOP
```

And the RAM contents of the DA-10 are accessible in the Intel-Hex format for further manipulation. Make friends with DA-10 and its simulation mode – you will not regret it. Besides, the DA-10 is also a complete data transmission and modem tester.



```
RUN  S SND RCV C1:     4 C2:    51
     D SND RCV C3:     0 C4:10001
T1:          52 T2:  309 T3:
**   Uhrzeit      11:24'51"N- 150

- $$$TEST-MESSAGE 0123456789 $

 $ --<$$$$$TEST OK $%>--$$$$TE

ST-MESSAGE 0123456789 $   $ --<$

                  █
$$$$TEST OK $%>-
```

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Circle 94 on reader service card

Computers

Price war shrinks home-computer profits

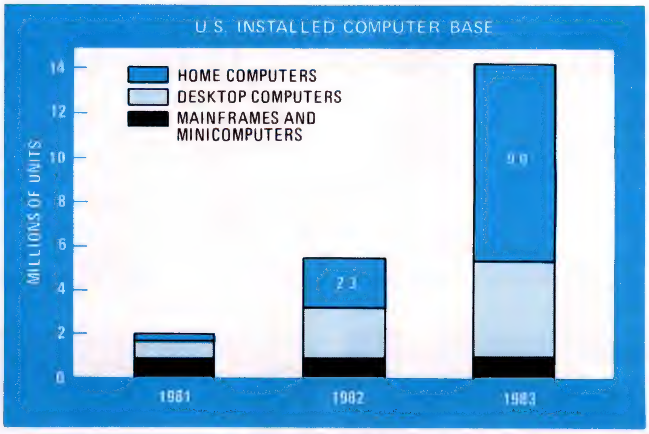
TI and Commodore go head to head as manufacturers hope for gains from software and peripheral sales; IBM waits in the wings

by J. Robert Lineback, Dallas bureau

The U. S. home-computer scene has turned into one of those good news, bad news stories just half a year after shoppers grabbed up nearly every unit made in the final weeks before Christmas [*Electronics,* Nov. 30, 1982, p. 48].

First, the good news for the recession-nagged electronics industries: despite some concerns that the buying spree would turn out to be a one-season phenomenon, retail sales have continued to climb well into 1983. Now for the apparent bad news: aggressive price cutting by market leaders currently seems to be taking much of the profit out of the sales.

That message came through loud and clear last month at Texas Instruments Inc.'s shareholders' meeting, where the competitiveness was partly blamed for a 74% drop in net income during the initial quarter of 1983. The Dallas-based firm is counting heavily on its 99/4A home computer to lead the way to higher 1983 corporate profits.



Fast growth. TI's market outlook, based on figures from International Data Corp., shows the home-computer segment of the overall market growing rapidly even as price cutting continues to eat into profits. TI partly blames the cuts for a 74% drop in its first-quarter net profits.

In the first quarter, TI delivered its millionth home computer, but it also suffered a major setback after discovering a potential defect in a transformer plug sold with the unit. Production was halted for an entire month. And now, new rounds of price cutting are expected to dull TI's second-quarter performance, says J. Fred Bucy, president.

Though likely to be much discussed at June's Summer Consumer Electronics Show in Chicago, pricing strategies are not the only issues facing U. S. producers. Market observers are awaiting the entry of a whole new breed of participants as the U. S. business grows.

Some entrants will come from traditional computer quarters. IBM Corp., for example, is reported to be studying a low-end personal computer, and analysts believe it could easily force a new market standard in the home segment. And some Japanese firms are expected to begin selling low-end units in the U. S. For example, Sord Computer Systems Inc. announced plans last fall to market its under-$250 M5 home computer. Also, Microsoft Corp. of Bellevue, Wash., is teaming with 10 Japanese makers to put together a worldwide software standard for under-$250 machines.

In addition, crowded video-game markets continue spawning new home-computer contenders as parents grow more concerned about how to instill "computer literacy" into their children.

Still, pricing remains today's dominant worry. In fact, a number of potential manufacturers have dropped or delayed product plans until the spiral ends.

Rebate battle. The price battle broke loose last August, when manufacturers began topping each other's consumer-rebate offerings to take market share in the final quarter of 1982. Unlike the more expensive, floppy-disk–based personal computers—where standard operating systems have emerged—each home-computer series is based on a proprietary architecture; owners of the under-$500 consoles must rely on the manufacturing source for most new software cartridges and peripherals.

With a larger customer base at stake, manufacturers are now gambling that lower profit margins today will translate into more lucrative follow-up sales tomorrow. Furthermore, many believe production costs will drop.

"This is most definitely an installed-base business, where it is the aftermarket rather than the frontier market that is at the core of these pricing strategies," explains Clive Smith, a senior analyst who tracks consumer electronics at The Yankee Group in Boston. For every dollar spent on the central processing console, Smith estimates, consumers today will spend one on software and another on peripherals.

Software question. Market analysts agree software profit margins are most se-

KENWOOD

An Indispensable Tool for Use in CD Player Development and Production

Dramatic developments in both lasers and sound reproduction technology have answered the dreams of audio enthusiasts in the form of a 12cm disc which can provide up to one hour of ultra high-quality reproduction using a non-contact technique which employs laser pickup of digitally recorded sound. The result is ultimate in high-quality music sources—the Compact Disc.

Trio has used its advanced compact disc player technology in developing a signal source equivalent to that derived from the laser pickup of a disc player. This signal source is the ideal tool for use in measuring the performance of such playback systems, and has been designed for easy incorporation into automated measuring systems using the popular GP-IB standard interface. The system consists of three units—the compact disc encoder, an A/D converter, and a digital I/O unit—which provide all the capabilities needed in both the development and production testing phases of compact disc players.

Compact Disc Encoder DA-3500 A/D Converter DC-3510 Digital I/O Unit DT-3520

FEATURES

- ★Generates a signal equivalent to that from the laser pickup of a compact disc player.
- ★Digital conversion of any analog signal is possible to the compact disc digital format.
- ★By using an audio processor, the various information, such as sub-code, required for EFM signals can be added, enabling the drive of a compact disc master laser cutting machine as well (Patent pending).
- ★In addition to processing of EFM and CIRC conforming to compact disc standards, generation of all the test signals required in inspection and testing of compact players is possible, as well as simulation of transmission systems.
- ★A 16-bit digital signal of high accuracy and low distortion can be generated to enable the measurement of compact disc player D/A converter and bandpass filter characteristics.
- ★A standardly provided GP-IB interface capability enables external control of all system functions, making this system easily adaptable to automated measurement systems and production testing applications.

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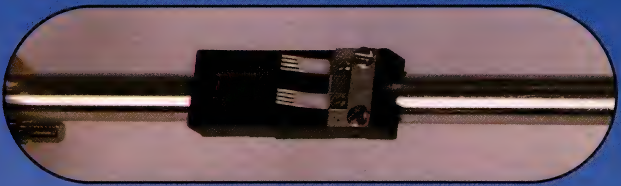

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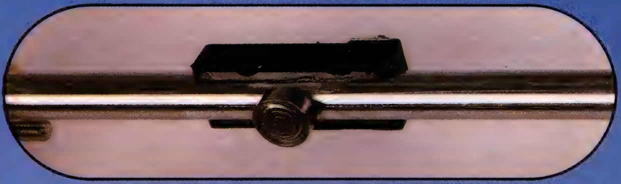

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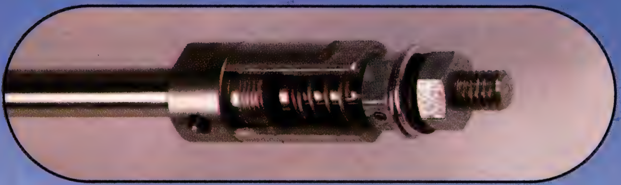

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cure; however, many question whether consumers are willing to invest hundreds of dollars in systems built around under-$100 computer consoles. "We are looking for a shakeout in this market," warns Norman Weizer, senior member of the consulting staff at market analyst Arthur D. Little Inc. in Cambridge, Mass. "This is going to be a market of who can stay in the longest, who is the best capitalized, and who is best able to generate volume."

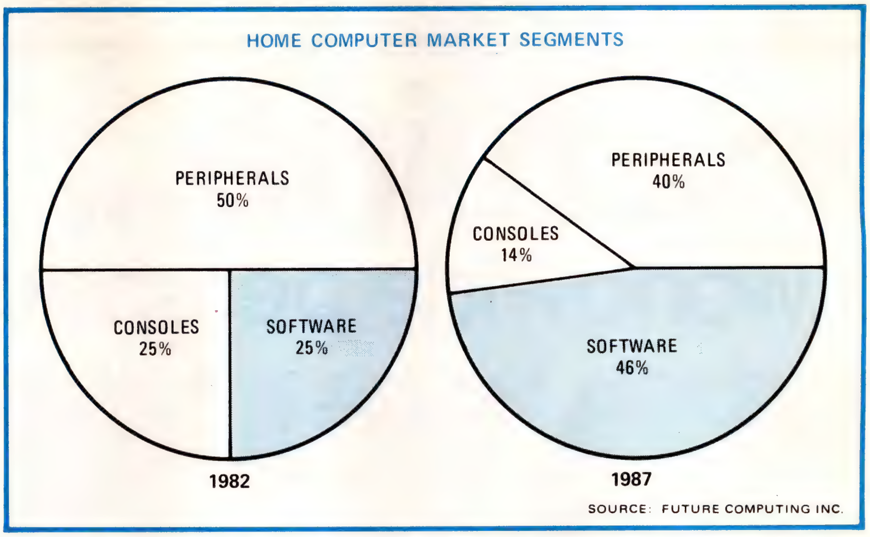
Weizer compares this new consumer-electronics segment to the development of the digital watch and calculator markets, both of which also rapidly became volume-driven businesses. "In some ways, it is the classical market situation," he observes, noting that, interestingly enough, TI has also been involved in watches and calculators.

Believing that what he terms a Hong Kong watch syndrome could set in at the console end of the business, Bill Ablondi, vice president at market researcher Future Computing Inc. of Richardson, Texas, thinks peripheral and software profit margins will continue to be attractive.

$8.2 billion. Future Computing estimates that the total U. S. market crossed $1 billion in 1982 and expects it to hit $8.2 billion in 1987. This year, hardware sales will double, with as many as 5 million consoles being sold, Ablondi projects.

Now, the issue is whether future price cuts will further accelerate buying. Ablondi believes not, pointing to what he considers a critical psychological barrier of $100 already broken by the two market leaders—TI and Commodore International Ltd. of Norristown, Pa.—and by Timex Corp. with its Sinclair machine.

But the biggest question among many market participants is whether TI or Commodore believes that. Commodore introduced its 8-bit VIC-20 computer in 1981 at a suggested retail price of $299. With the latest round of price cuts and retail store discounts, a VIC-20 with 5-K bytes of random-access memory can cost less than $90. Commodore has also begun offering $100 credit for trade-ins on its higher-end 8-bit model 64, whose suggested retail price with 64-K bytes of RAM is $595.



SOURCE: FUTURE COMPUTING INC.

Switch in emphasis. With a large customer base in place, manufacturers hope that less profit on consoles today will mean more in the aftermarket tomorrow.

Lower than low. TI's 16-bit 99/4A, introduced in 1981 at a price of $525 with 16-K bytes of RAM, will cost less than $100 after June 1 once a $50 rebate program begins. That summer street price is much lower than TI officials were projecting in January, when the firm's Consumer Group unveiled the 99/2—what was then promoted as the world's first under-$100 16-bit computer. With the more powerful 99/4A to be sold for less than $100, the future of the new low-end TI unit is cloudy.

TI is expected soon to introduce the 16-bit 99/8 [*Electronics*, May 5, p. 41], which will attack the same customer base as the Commodore 64. To counter, Commodore has disclosed plans to make an 8-bit model 128/80, which will have 128-K bytes of RAM and cost $895. The firm, which recently negotiated a deal to use Zilog Corp.'s 16-bit Z8000 microprocessor, is also working on a model 256 with even more internal memory. By year's end, most market analysts expect price-cutting skirmishes also to erupt in the market for $500-to-$1,000 home computers.

For the most part, the TI-Commodore tug of war has left the market in a confused state. Timex, which was the first to offer a computer for less than $100 last year—the Sinclair ZX-81—has trimmed the price of the unit to less than $50. Losing business to the more powerful TI and Commodore units, Timex plans soon to market Sinclair's newest design, the Spectrum, which will be sold as the model 2000 for $149.95 in its 16-K version and $199.95 for the 48-K one.

Atari ready. Also, after months of waiting, Warner Communications Inc.'s Atari operation is expected to drop its premium-pricing scheme and begin chopping at tags. Already, Atari—which announced last February it would be moving its computer operation to Asia to increase profitability—is offering a $50 rebate plus $50 worth of free software on its low-end model 400 with 16-K bytes of RAM. It retails for $299.

A less aggressive pricing strategy may cost market share, but not necessarily profits, says Ed Juge, director of Radio Shack computer merchandising at Tandy Corp.'s headquarters in Fort Worth, Texas. By most estimates, Tandy's share of the home-computer business has slipped from No. 1 or 2 in 1981 to as low as No. 5 in 1983. However, Juge maintains, volume is growing.

"I think we will probably see this [price war] continue until the guys involved get tired of it," says Juge, adding that his firm will continue to trim prices as production costs drop. In what is being called a scheduled promotion, Radio Shack is reducing the price of its 8-bit TRS-80 Color Computer (with 16-K bytes of RAM) by $100 to $199 in May and June. "We have no intention of trying to gain quick market share at the expense of making money," he says. ☐

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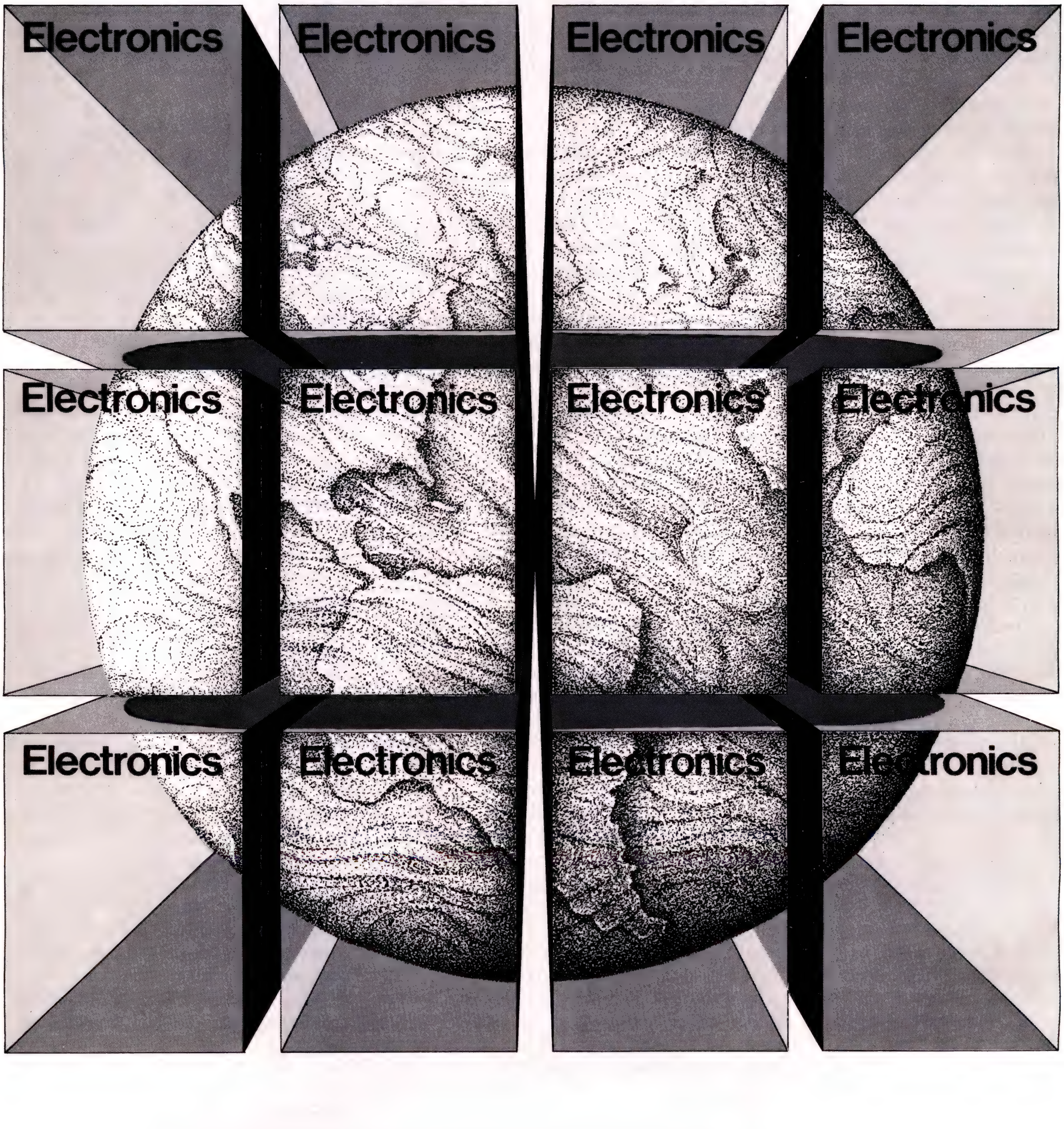

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Packaging & production

Packaging rules components conference

VLSI cast its shadow at Electronic Components Conference, with papers on new materials, packages, and bonding methods

by Jerry Lyman, Packaging & Production Editor

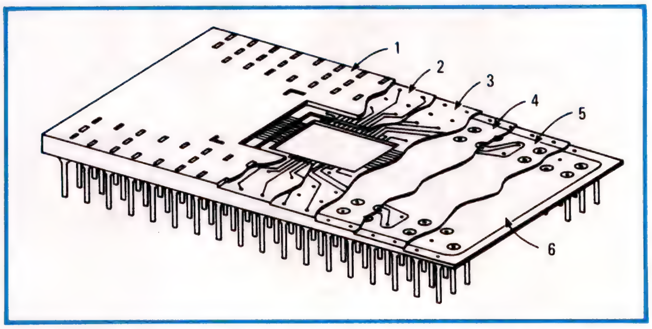
The added importance given packaging and interconnection in the era of the very large-scale integrated circuit has been reflected in their growing prominence at the Electronic Components Conference. The meeting, whose stated aim is to present new developments in electronic components and hybrids, has been augmenting its traditional sessions with others on package design, bonded interconnections, packaging technology, surface-mounting technology, and related subjects.

In fact, about 60% of all the papers presented at Orlando, Fla., this week fell outside the stated aim of the conference. The results of this infusion were papers on such leading-edge subjects as a new glass-ceramic substrate with a low firing temperature that is intended for high-speed, dense, multilayer substrates; a pin-array VLSI package; and tape-automated bonding for devices with many leads.

The glass-ceramic substrate was described by seven researchers from Japan's NEC Corp. in a session on packaging technology. One of the outstanding papers of the conference, it points the way to a method of surmounting speed limitations inherent in present-day multilayer hybrids.

The common way to make complex hybrid circuits is with stacks of ceramic-alumina green sheets that have molybdenum or tungsten conductors screened on and are fired at 1,500°C. The material's dielectric constant is about 10, and its temperature coefficient of expansion roughly twice that of silicon.

However, the relatively high resistivity of the refractory metals used limits the fineness of the lines that can be screened; moreover, it is difficult to form small holes, known as vias, in the ceramic. Those two limitations not only curb packing density and fine patterns and contribute to long conductor runs, but combine with the high dielectric constant to delay propagation excessively.



Six planes. Plane 1 in Bell's package has guide marks; 2 and 3, cavity and wire-bond fingers; 4 and 6 are ground planes; 5 is a power plane.

Beats alumina. The NEC presentation described its newly developed glass-ceramic substrate that overcomes many of alumina's limitations. The material, a mixture of alumina powder and lead-borosilicate-glass powder, has an optimum firing temperature of about 900°C. Its dielectric constant is a low 7.5, and with a TCE that is 10% greater than that of silicon, it offers a good thermal match between substrate and chips.

NEC's multilayer glass-ceramic substrate has gold- or silver-palladium alloys screened on for its circuit patterns, permitting a designer to work with lower-resistance fine-line conductors. In a laboratory model, the material was used to build multilayer substrates for a computer system that contained multichip packages. Vias with 100-micrometer diameters and 100-μm conductors on a 200-μm grid were produced in the substrates.

Also, in another development, the NEC team said that it was possible to punch as many as 110,000 vias in a 120-millimeter-square green sheet. The new material, they concluded, appears to be capable of both high performance and dense packaging and interconnection.

Some of the experimental substrates produced at NEC used TAB chips, a technique that some predict will be the package of the future for VLSI. In still another important paper from Japan, three scientists from Hitachi Ltd. discussed in the session on bonded interconnections how to apply the TAB technique to chips with high lead counts.

Problems of TAB. The paper's authors, T. Kawanobe, K. Miyamoto, and M. Hirano, noted that present TAB technology is fairly similar at many firms—a combination of gold bumps on the chip and tin-plated copper tape are eutectically bonded together. That technique works well when the lead count is low, but for a chip with many input/output pads, there are three major problem areas:

- The protective glass film of the chip can crack because of the higher pressure and temperature involved in bonding a larger number of leads.
- Short circuits can form between a bump and a chip edge because of a gold-tin eutectic lump.
- Tin whiskers can give rise to short circuits between

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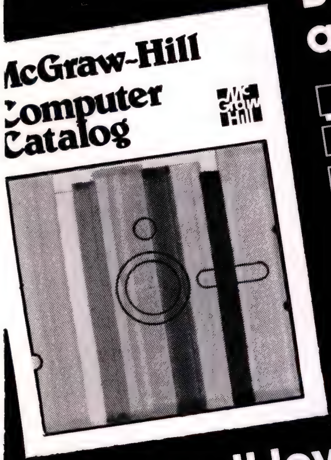

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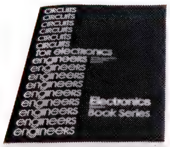

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adjacent leads on the tape.

Hitachi's engineers came up with a new TAB structure in which a layer of polyimide film over the glass layer keeps the glass from cracking during bonding. Bump and chip short-circuiting are prevented by switching to a tin-capped gold bump and a copper tape thinly plated with gold. Nicely enough, such a gold-plated tape also eliminates the growth of the whiskers.

Rearranged pins. Another standout paper on packaging was put together by C. W. Deish and J. F. Gogal of Bell Laboratories in Naperville, Ill., and Murray Hill, N. J., respectively, and J. W. Stafford of American Bell Inc. in Holmdel, N. J. In a presentation in the conference's session on packaging design, the researchers described a pin-array package that is rectangular like a dual in-line package, but otherwise substantially dissimilar: the new package's I/O pins do not fully populate the base but instead are arrayed in three rows on 100-mil centers along each long side.

Made of cofired tungsten and metalized ceramic with 104 I/O pins, the package measures only 1.16 inches wide by 1.88 in. long. Dual-tier wire bonds serve to cut down wire-bond lengths, which in turn enhances electrical performance. One of the package's more impressive advantages is that it can be mixed with high–lead-count DIPs on large printed-circuit boards.

The Bell researchers say that the package is to be used in systems where many leads must switch simultaneously onto a heavily loaded bus. But because such switching may result in considerable electrical noise, the package has to have the lowest possible ground impedance. This is accomplished by committing 20% of all pins to power and ground and by strategically positioning them on the package.

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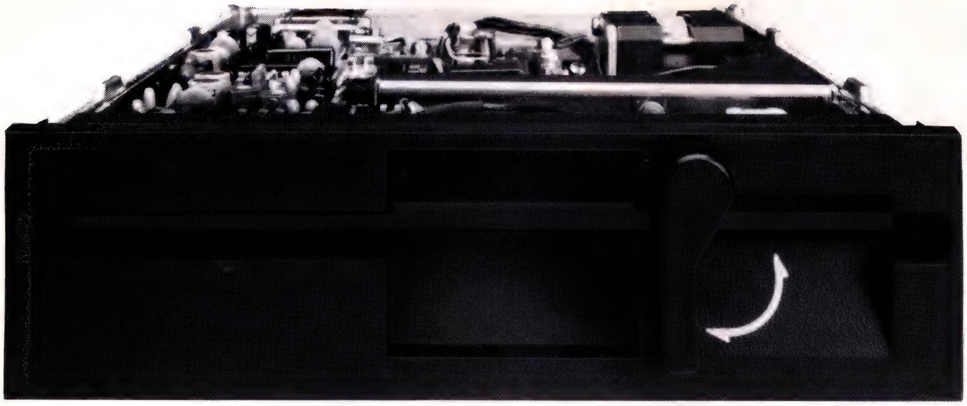

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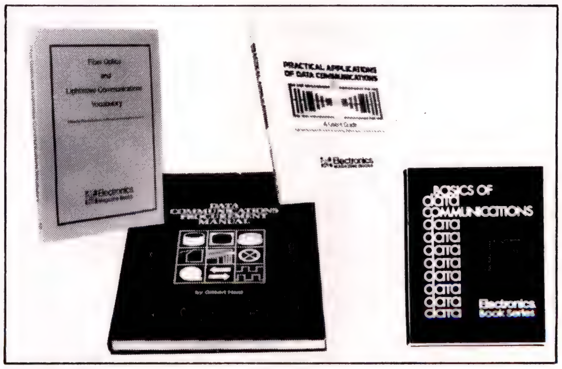

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Electronics abroad

French plan reaches critical point

Two of the three nationalized electronics conglomerates are in the red as government reexamines its overall approach

by Robert T. Gallagher, Paris bureau manager

Just 15 months after France's Socialist government appointed chief executive officers for the country's nationalized electronics industry, all those involved are weighing decisions that could well determine the success or failure of that entire nationalization operation.

At the moment, two of the companies concerned, Thomson-Brandt and CII-Honeywell Bull—the third is Compagnie Générale d'Electricité—are bathing in a flood of red ink that is menacing the government's entire industrial strategy. Both government and industry officials say that they are pinning their hopes on consumer electronics, telecommunications, and data processing to complement the military electronics area that has always been a profitable French forte. Another key will be the long-awaited components plan from the research and industry ministry.

Both government officials and industry executives emphasize that the relationship between the government and the nationalized companies is the standard one of a stockholder to a company in which the stockholder owns a majority interest. Moreover, they add, the companies are autonomous so long as their strategies do not come into conflict with any governmental priorities—chief among which, they add, is that the nationalized electronics companies be competitive and profitable.

Big loser. Thomson-Brandt lost a massive $280 million in 1982 in components, medical electronics, telecommunications, and carry-forward losses, enough to justify an extensive restructuring. President Alain Gomez has already begun that task and says, "Our markets are consumer electronics and detection and arms systems, in addition to the necessary components for those products. Everything else is debatable."

The first step in implementing this strategy was an attempt to take over Grundig AG, West Germany's largest consumer electronics group. When that failed, Thomson bought the Telefunken subsidiary of West Germany's AEG-Telefunken and signed an extensive licensing agreement with Victor Co. of Japan (JVC) under which Thomson will be able to produce video-cassette recorders. Left in question, however, are the company's activities in telecommunications and medical electronics.

Gomez tried to plug the medical-electronics gap with an agreement to jointly develop radiological and medical imagery equipment with Technicare Corp., Solon, Ohio. Thomson would have been permitted to market the equipment in Europe, with the American company retaining exclusive rights in the U. S. market.

Solution sought. Nonetheless, the government thought that the accord, by cutting off the American market for a range of strategic products, would keep the medical electronics subsidiary small, "so we asked Gomez to come up with a different, more suitable solution, and that's what he's in the process of doing," says a government source.

Telecommunications promises to be an even stickier area, because it is considered strategically important by the government. Three nationalized companies, CGE subsidiary CIT-Alcatel and the Compagnie Générale de Constructions Téléphoniques, a for-

French pin their component hopes on two firms

When the French components plan is finally announced, it will revolve around two axes: Thomson-CSF Composants and Matra-Harris Semiconducteurs. Thomson has never made money in integrated circuits and refuses to discuss its plans. But industry sources feel that the only significant change will come in its MOS lines, with its Grenoble-based Thomson-Efcis being used to produce small quantities of circuits for the company's military electronic systems and with its newest operation—Eurotechnique, the company near Aix-en-Provence that was formerly 49% owned by National Semiconductor Corp.—set up to handle volume runs. National has reportedly proposed to share research and development with Thomson on products like erasable programmable read-only memories and static random-access memories.

On the other hand, Matra seems to have a clearer sense of direction, working with variations of Harris technology to fill niches in the gate-array, microprocessor, and telecommunications fields. The company has a joint design venture with Intel Corp. that gives it access to the U. S. company's n-channel MOS library. Though only some three years old, it expects to be out of the red soon. Also, it is satisfied with how it performed in the recent bad years for the components industry in general, which were worsened by a rising dollar that made investments in U. S. equipment far costlier than at contract time.

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mer subsidiary of International Telephone & Telegraph Corp., in addition to Thomson, are involved in both public and private telephone switching. According to some industry sources, Gomez would prefer to simply get rid of the business.

The snag is that within the company, Thomson needs telecommunications expertise for its military activities, and the government is determined to have two companies in public switching. But the ailing CGCT is too weak to be one.

One too many. "The decisions that will shape the French telecommunications industry are in the process of being taken, but what is clear is that three systems are too many for a country the size of France," asserts Jean-Claude Hirel, director of the Direction des Industries Electroniques et de l'Informatique, the electronics arm of the research and industry ministry. "Finally, there will be only two systems."

Most industry observers expect this to mean that the CGCT will be given the task of using its facilities to produce the Thomson system, while itself specializing in private telephone systems. This, however, is unlikely to be enough to turn the Thomson operation around, a project the company says it is working on though it refuses to discuss details.

Paradoxically, one company for which Thomson's success in telecommunications seems important is competing CIT-Alcatel. "The last thing that the reorganization of the country's telecommunications industry should result in is something that looks like 'Téléphone de France,'" argues Pierre Chavance, the firm's managing director. "We can be far more effective in international competition operating as CIT-Alcatel."

Sales abroad. The international market is an important profit base for CIT-Alcatel, which exports some 30% of its $1.8 billion total sales. According to Chavance, the company's objective is to export 45%, a fact that would bode well for its digital switching operation, an area in which it already commands 35% of the world market.

Another turnaround necessary for the overall success of the nationalization plan involves data-processing specialist CII-HB. After a loss of some $200 million in 1982, the company will receive a much needed injection of capital, more than $1 billion over the next four years.

"This company has received no new capital since 1978, and in a business where it takes as much money as it does to grow in data processing, that's a disaster," says Jacques Zyss, director of strategy and planning. "Unlike military electronics, telecommunications, and components, where manufacturers have received the benefit of large investments for research and development, we've gone pretty much neglected," he says.

New look. According to Zyss, CII-HB will undergo an ambitious reorganization program to become a holding company with four subsidiaries, one each for large systems, minicomputers, office automation, and peripherals. Though the company's strategy has been criticized as too broad-based and ambitious, Zyss responds that CII-HB has no intention of doing everything itself and will share the burden with partners in such areas as distributed data processing

If the nationalizations fail, and French government officials and executives in the nationalized companies unanimously measure success in terms like market share and profitability, it will not be for lack of investment. "The government is now the major shareholder in these companies, and we intend to fulfill our responsibility of shareholder," says the DIELI's Hirel, who will oversee the distribution of much of the roughly $20 billion that the government will invest in its electronics industries during the next five years.

But with so much red ink around, some wonder if the francs will be distributed equitably. "The government must resist the temptation to concentrate too much on those companies with deficits while ignoring those that are profitable," says Georges Peberau, managing director of the very profitable CGE. "But I sincerely hope, and believe, that this kind of policy will be avoided."

But, counters one government official, "it is true that that is a temptation. But that's why we are here, to make sure that it doesn't happen." ☐

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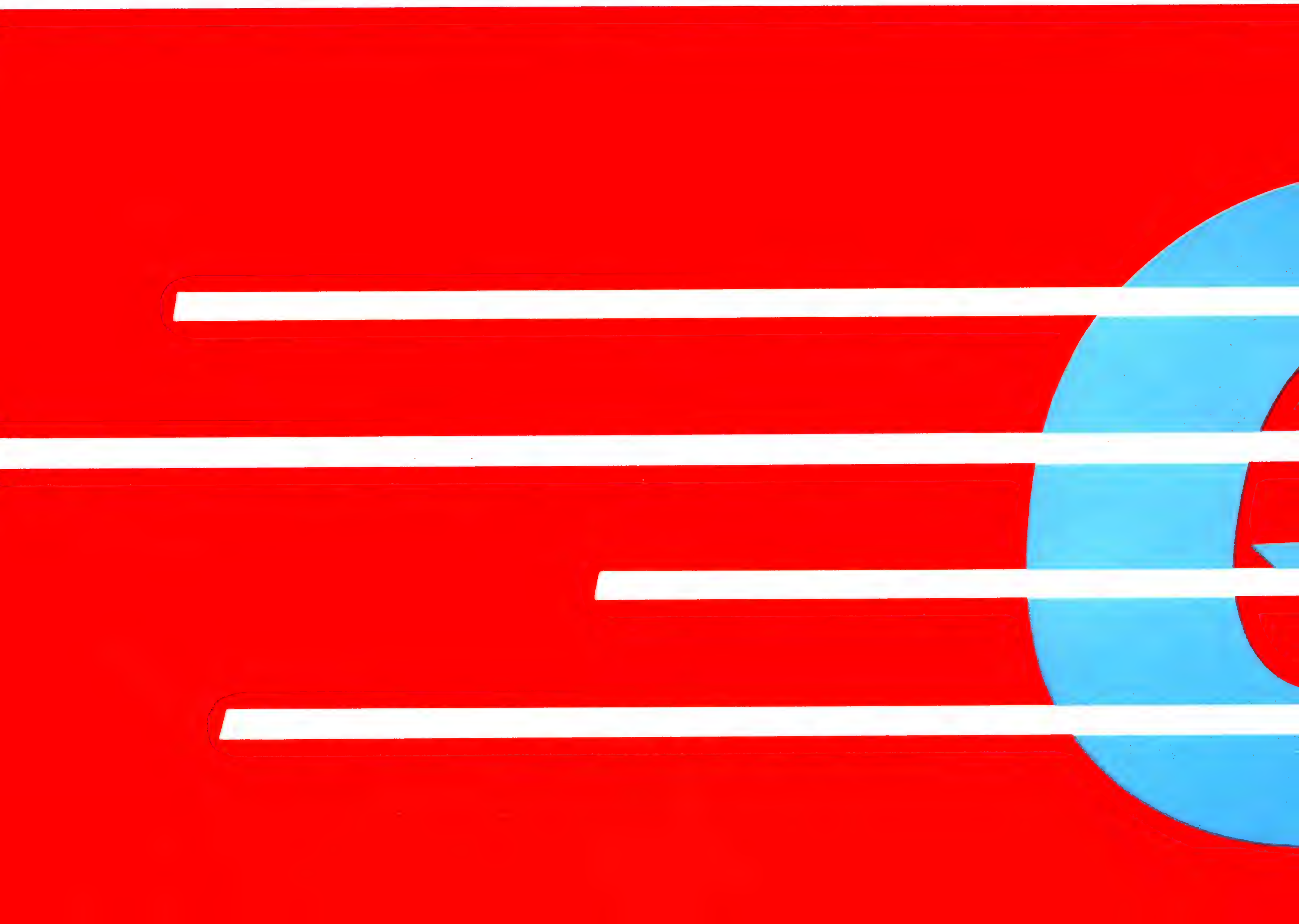

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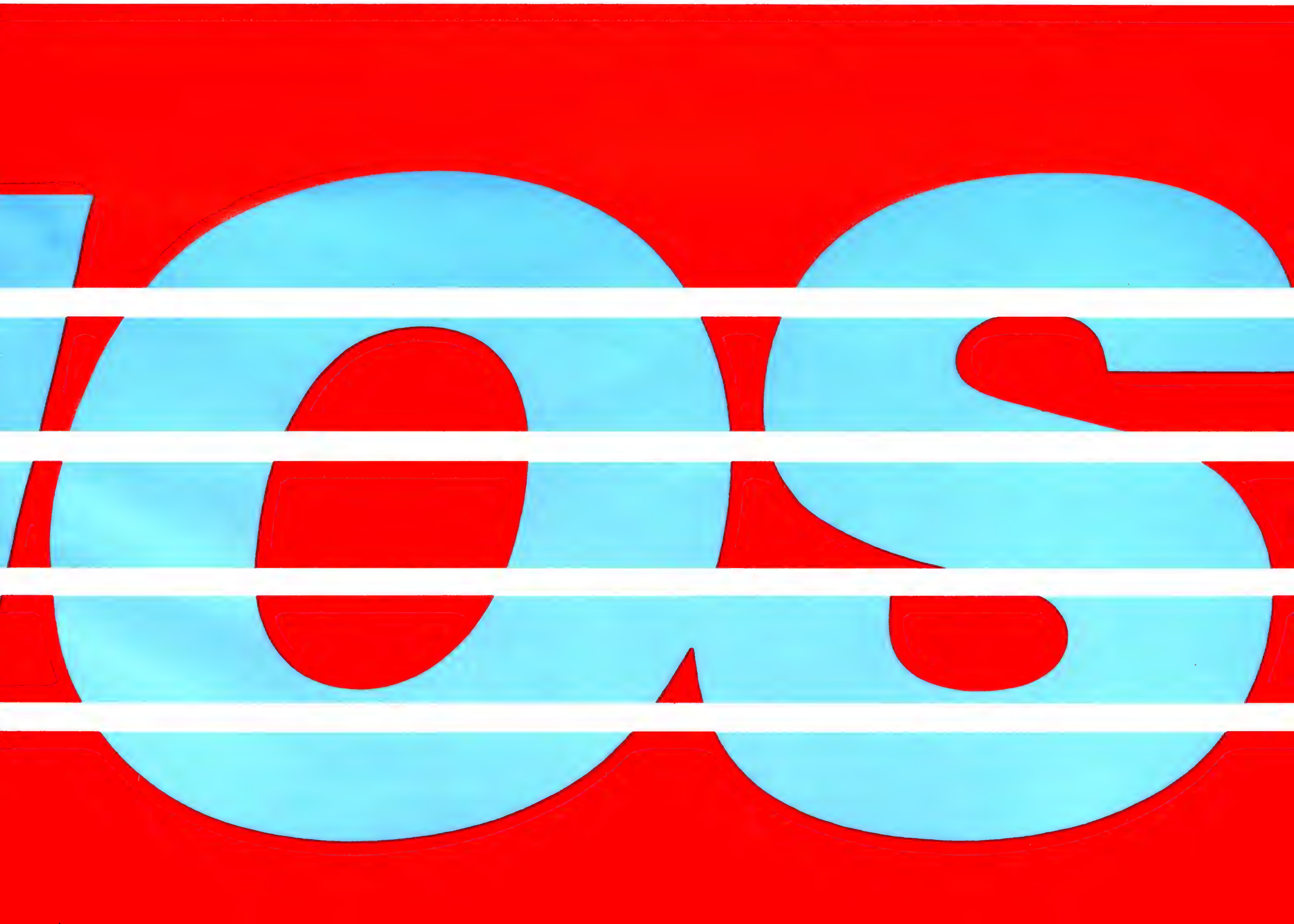

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533E	■	■	Octal Transparent Latch, Inverting, 3-State
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85E	■	■
86E	■	■
107E	■	■
109E	■	■
112E	■	■
123E	■	■
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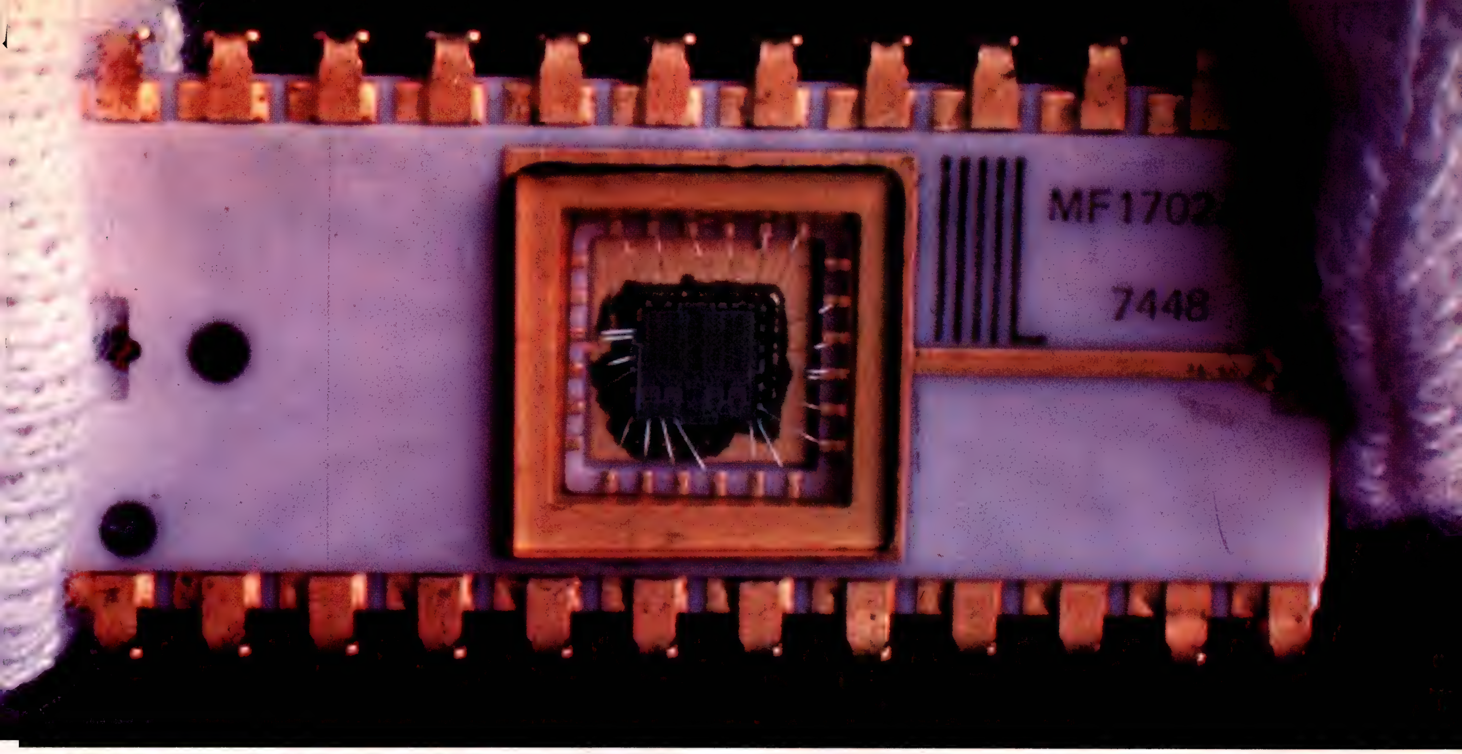

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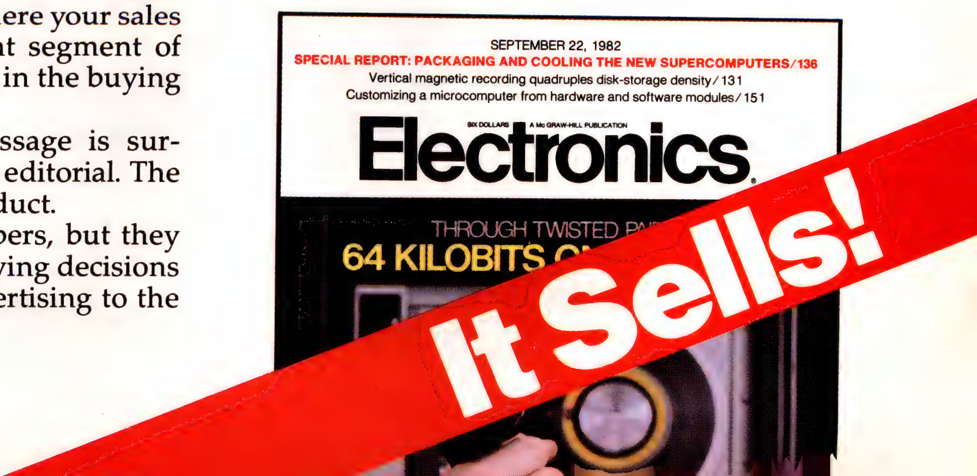
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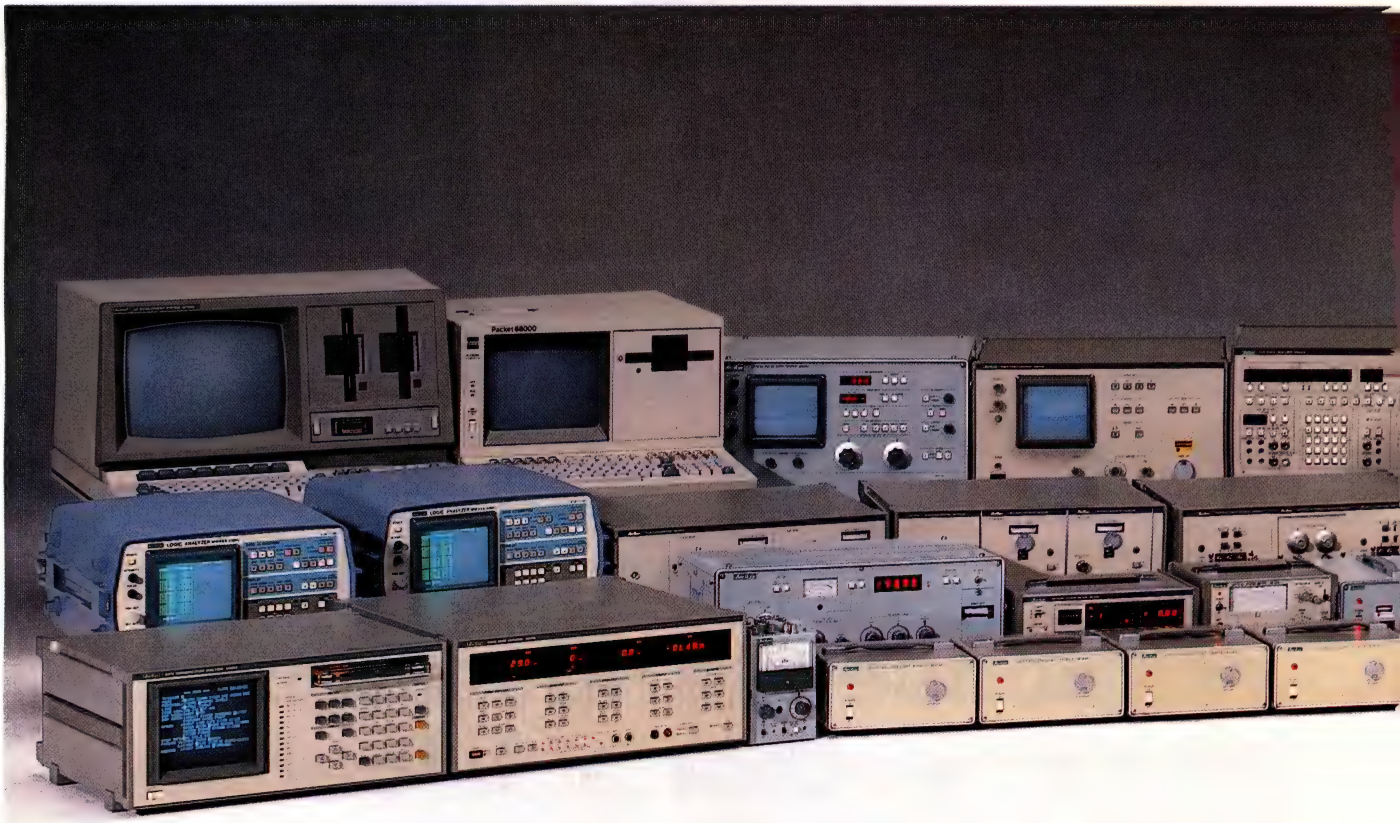

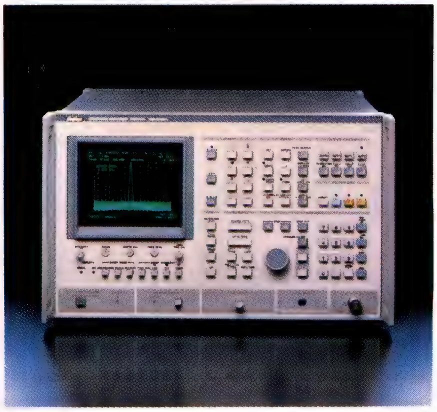

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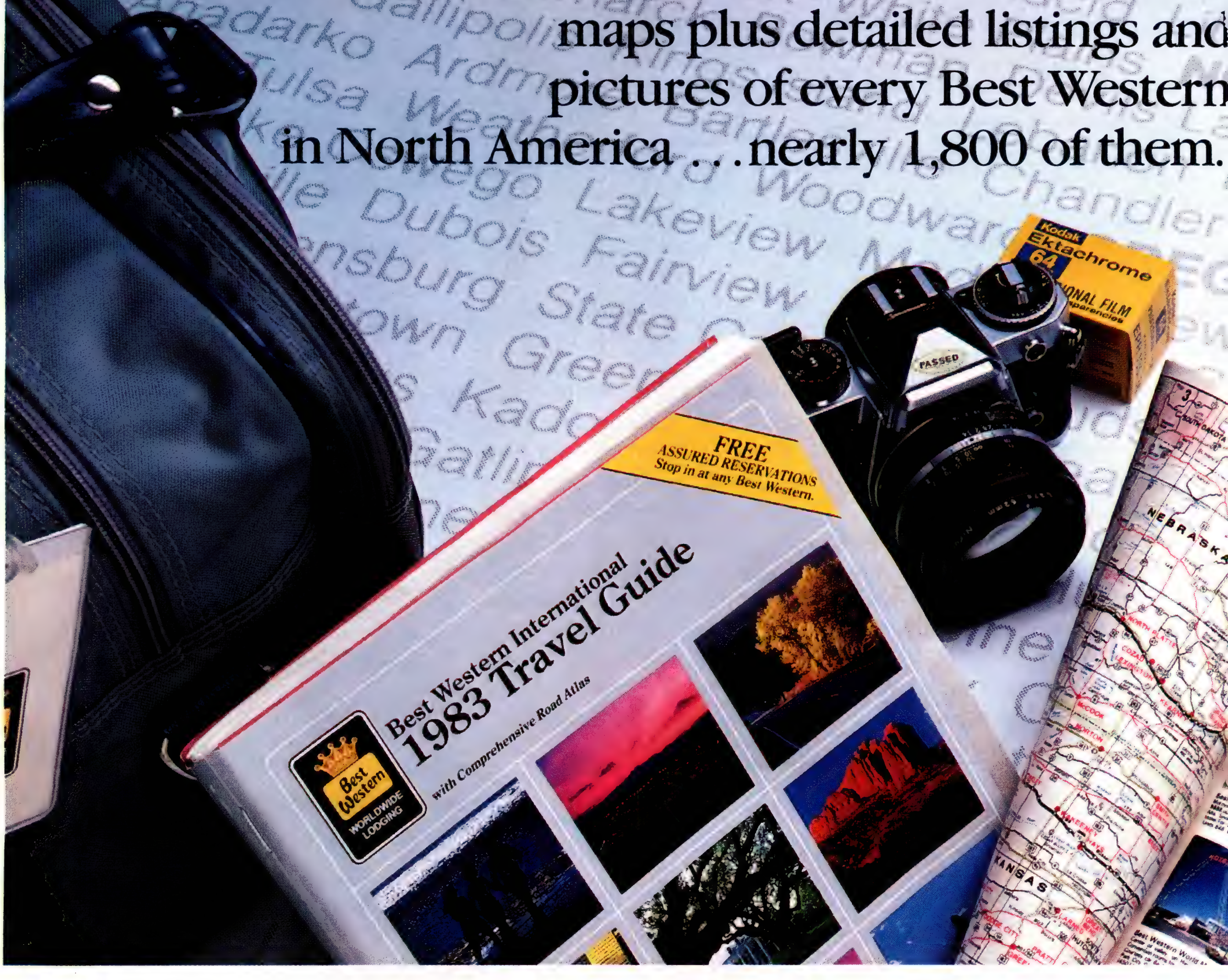
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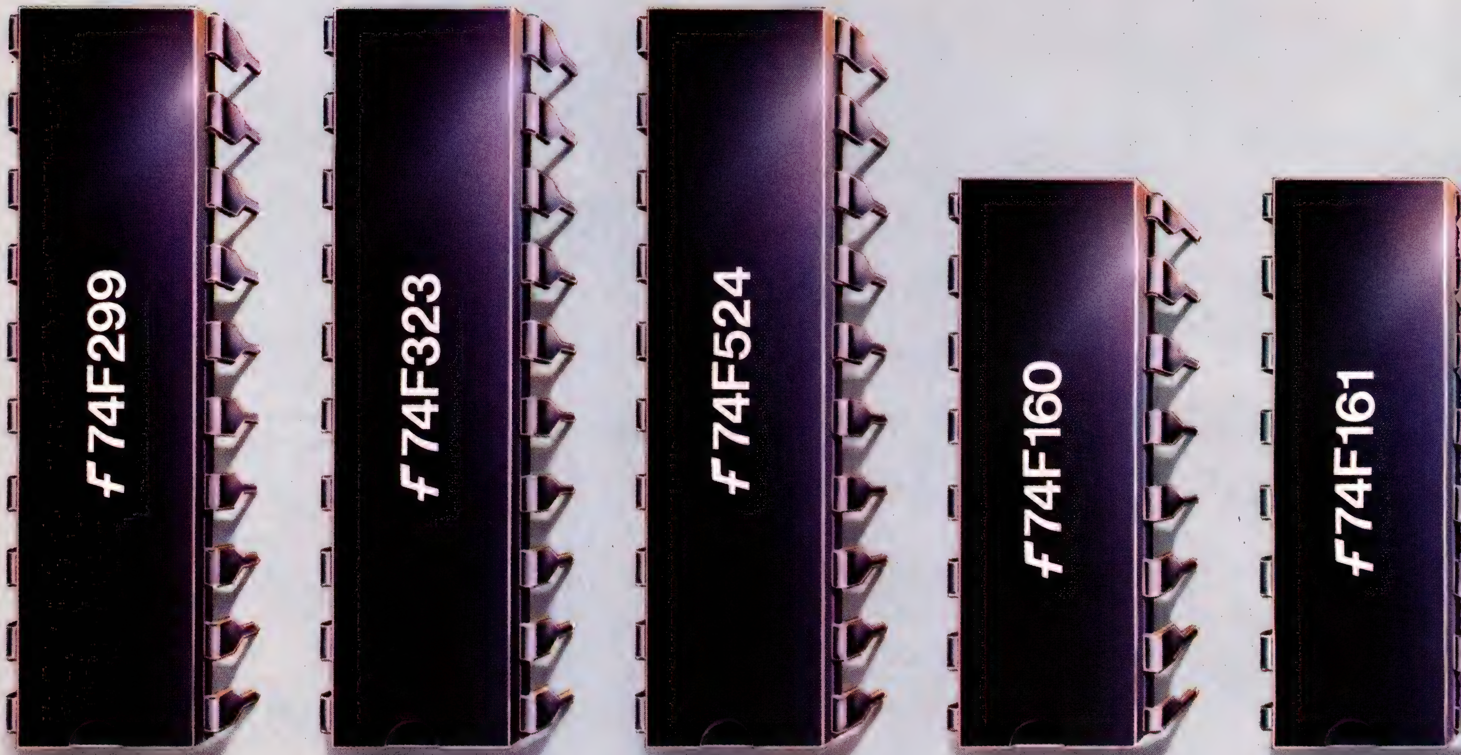

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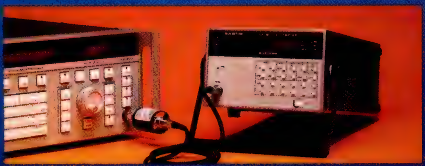

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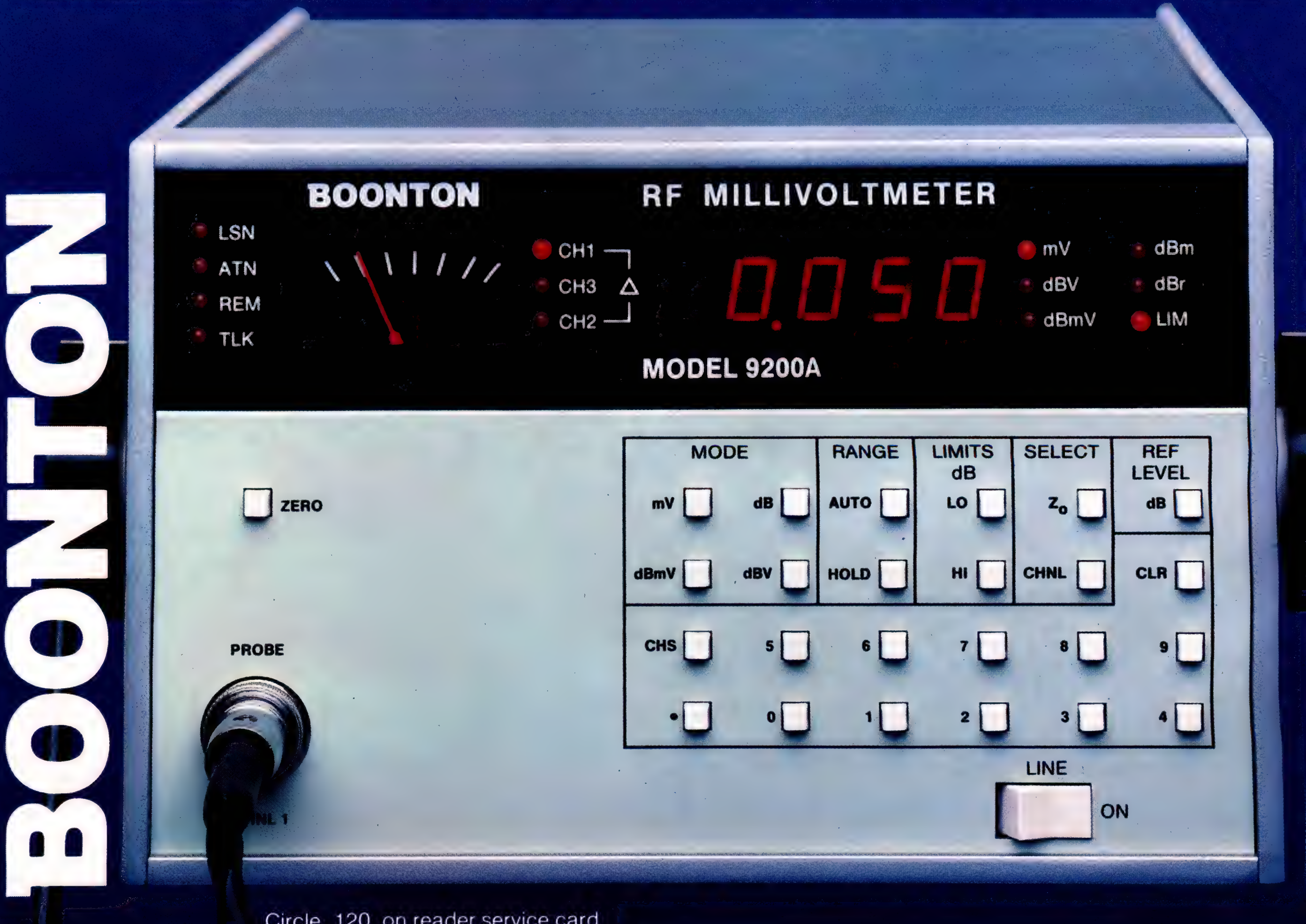

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ALU, multiplier chips zip through IEEE floating-point operations

Pipelined multiplier crunches 32-bit multiplications at 5 megaflops; separate ALU chip handles addition, subtraction, and normalization

by Bob Woo, Lyon Lin, and Robert E. Owen, *Weitek Corp., Santa Clara, Calif.*

☐ Once confined largely to batch processing on mainframe computers, floating-point computations are migrating to smaller systems for such applications as seismic processing, medical imaging, and model simulation. To date, however, system designers hoping to exploit the precision and dynamic range of floating-point processing have been forced to use either fast but expensive array processors or low-cost but slow coprocessors—or even to build their own hardware subsystems.

Now, though, an attractive alternative arrives in the form of a pair of chips (Fig. 1) capable of churning out 5 million 32-bit floating-point operations a second in the standard format proposed by the Institute of Electrical and Electronics Engineers and designated IEEE standard 754. Among the choice of arithmetic functions possible, those most frequently encountered in high-performance systems are add, subtract, multiply, and floating-point-to-integer conversion. Functional partitioning of the chip set separates these functions roughly equally into a multiplier and an arithmetic and logic unit. (The less frequently used floating-point division can also, if needed, be performed in a two-step algorithm with a multiplier and ALU.)

Using a standard 3-micrometer n-channel process, the WTL 1032 multiplier and WTL 1033 ALU fit on dice measuring respectively about 300 by 290 and 305 by 225 mils on a side. Smaller than most floating-point coprocessors, these sizes ensure high-yielding commercial parts, not just captive-user technology show pieces. As for other practical considerations, the low power dissipation of 1.5 watts typical of each chip reduces cooling needs and also permits use of smaller packages like the 68-pin leadless chip-carrier, among others, in addition to the usual 64-pin dual in-line package. Also, the pinout common to both chips provides circuit-board layout advantages regardless of whether the chips are paralleled or cascaded as multiplier and accumulator.

These new floating-point components and the IEEE standard are attractive not just for new floating-point applications, but also for more established real-time control and signal-processing applications that till now have been forced to settle for integer arithmetic. In such applications, the arithmetic precision must also be high—20 to 24 bits—to maintain stable operation and provide the high signal-to-noise performance possible with digital solutions. Speed is of course not just a convenience but a vital necessity to the correct operation of such real-time applications. Often processors are arranged in parallel or cascaded together in order to furnish the needed processing power.

Integer deficiencies

In typical real-time systems today, dynamic range and precision have had to be restricted because of the use of an integer implementation. At that, only 16-bit parts have been available with the speed or any of the size and cost benefits of very large-scale integration. The severe performance compromise that such a situation causes hurts all the more because it is common practice to simulate and develop the systems first of all on floating-point array processors.

Transporting this type of system to a manufacturable solution then often involves extended development time and painful redesign of the algorithms in order to recover lost performance. The IEEE single-precision floating-point format with its 24-bit integer significand and 8-bit exponent—providing a dynamic range of over 1,500 decibels—satisfies the high-precision requirements and wide dynamic-range needs of these real-time applications.

For all applications, compatibility with the IEEE standard can improve the transportability of working solutions and speed the availability of products. Floating-point arithmetic does require more operations and take more time; however, in almost all interactive and real-time applications, data is processed as vectors, so that pipelining can be exploited to maintain the high data throughput that has previously been achieved by means of integer arithmetic.

Standard environment

Although the standard defines a complete programming environment, the choice between hardware and software functions is left to the implementor. Integrated circuits like the 1032 and 1033 contain only basic arithmetic functions, so that they cannot be said in themselves to conform to the standard for those functions, but rather to be merely compatible with it. Nevertheless, they must contain the complementary hardware functions if they are to implement the entire standard. In general terms, compatibility means using the standard's format, its special values, its arithmetic, and its methods for handling exceptions or errors.

In the format specified for single-precision 32-bit values, a variety of entities are defined (Fig. 2). Besides zero and unique representations of plus and minus infinity, the standard defines a range of bit patterns that do not represent numbers at all. Such a so-called not-a-number (NaN) can be used for communication. It should be noted that the most significant bit of the significand—called the hidden bit since it is not physically represented—is always 1 except when the value represented is 0 or a denormalized (or underflowed) number, in which case the hidden bit is always 0.

Arithmetic operations are defined for all values except for NaNs. Retaining denormalized-number arithmetic yields a gradual loss of significance for underflowed results. All numeric results are calculated to the highest possible precision and then rounded to the precision of the format. Even the methods of rounding and handling representations of infinity are specified. In each case, a default method is given, as well as options desirable in certain applications—for example, rounding options used in format conversions.

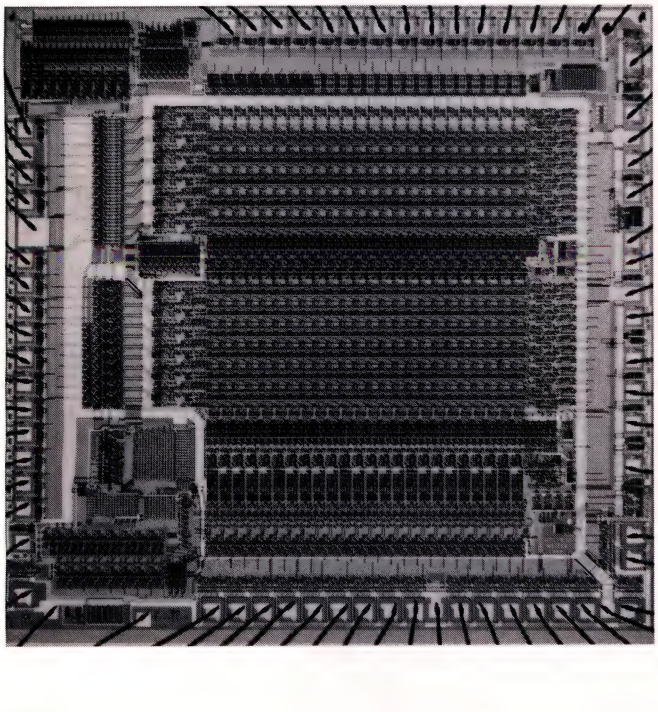
Rounding to the nearest number, or nearest even number if it is a tie, is specified as the default rounding procedure in the IEEE standard. This option will be preferred for most applications because of its decreased bias in the resulting values, but rounding toward 0 or plus or minus infinity may be selected.

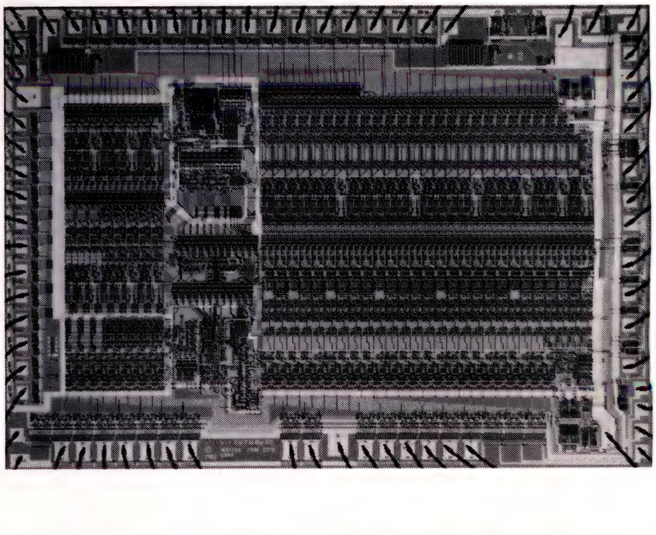
Valid and invalid

Only normalized floating-point numbers are considered valid by the standard, and any denormalized (underflowed) number must be flagged as an exception. However, these denormalized numbers must be preserved and the arithmetically correct—though perhaps misleading—result produced. This is called gradual underflow.

When the ALU chip performs this arithmetic, it normalizes the numbers by allowing the biased exponent to roll under or wrap around, treating it as a 2's complement negative number. After the ALU operation is complete, the result is denormalized and flagged. These additional steps are easily done with the existing significand shifters and exponent incrementers and decrementers needed for normalized floating-point addition in the ALU.

These functions, though, are not needed for normalized floating-point multiplication and are not used enough on denormalized values to justify their inclusion on what is already the larger multiplier chip. Rather, denormalized operands for the multiplier are flagged and returned to the ALU, where they are normalized with a





1. Megapower. Using a standard 3-μm n-MOS process, the WTL 1032 (left) handles 5 million floating-point multiplications a second in its 300-by-290-mil^2 area. Its companion chip, the WTL 1033 ALU (right), manages additions and subtractions at the same rate within its 305-by-225-mil^2 size. Each chip dissipates only about 1.5 W.

negative exponent. These wrapped numbers, with wrapped-around exponents, are then returned to the multiplier. This is a time-consuming procedure and one that in many real-time applications is not necessary. In these cases, substituting 0 for the denormalized operand produes a valid result of 0, and processing proceeds. This option is included in the multiplier and is invoked by choice of the fast mode of operation in its mode register.

Errors and exceptions

Additionally, the format specifies a uniform detection and treatment of errors or exception conditions. Invalid numbers and operations that arise in floating-point arithmetic are detected as exceptions and must be handled in either of two ways, according to the standard.

Case one, the default case, must flag five separate conditions and produce specified results. These exceptions include invalid operands, underflow, overflow, inexact results, and division by 0.

Each of these exceptions must result in certain default numerical results, like infinity at overflow or denormalized numbers at underflow. For data-path components, flagging the exceptions in a status register and returning the correct default result is all that is necessary. The four standard exceptions that apply to these chips (division by 0 does not apply) are output in a 3-bit status format. An additional exception handled by the multiplier is denormalized input. This exception detects the denormalized operands, which must be returned to the ALU unless the fast mode is enabled.

In the second case, user-written software routines must be able to attempt recovery of data as it existed before the exception occurred. NaNs can be helpful in this recovery process. Exception-detection logic must be present in the data path so that default results may be generated and exception flags set. Since the actual handling of the exception trap is defined by the designer, only the simplest control structure in the chips is desirable for maximum flexibility and speed.

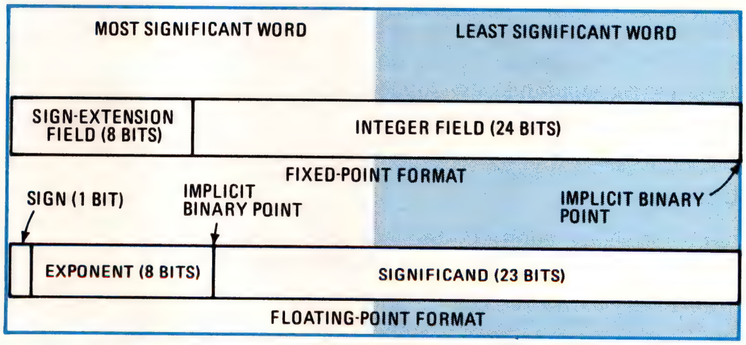
Speed is an important requirement of most interactive applications. For high-resolution shaded graphics displays, systems churn through many millions of floating-point operations a second. Such megaflop rates are needed to maintain system response times at a level acceptable to the display user working with normal multi-operation commands. Simulations are similarly demanding because of the large number of data points and the fine resolution required to generate the needed results.

All logic is static, so any clock rate from dc up to 10 megahertz may be used. Propagation time through a pipeline stage is a maximum of 200 nanoseconds. Thus, two full 32-bit input operands can be loaded and one 32-bit result unloaded every 200 ns, keeping the pipeline full. This corresponds to a 5-megaflop rate for each chip. Total latency time from the entry of the most significant operand word on the chip to the delivery of the least significant result word is a maximum of 1.1 microseconds. In a special flow-through mode, the total latency period undergoes a reduction to 900 ns.

System effects

These high individual component speeds become high system data rates in a variety of different data-path configurations. In a more limited-function real-time signal processor, like those used for communications, the ALU and multiplier are more often placed in a serial pipeline. But in programmable array processors, the ALU and multiplier are likely to be paralleled on two data input buses and one output bus connected to registers or memory. With 32-bit-wide buses and with the individual microprogramming of each chip commonly used, such a configuration produces a 10-megaflop pipelined rate. This same 10-megaflop rate may, moreover, be multiplied by splitting the data samples among two or more pipelines—a feasible solution because of the small size of the arithmetic elements in this case.

More conventional central processing units are likely to configure the ALU and multiplier in parallel also, but on one or at most two buses. The buses may be limited to 16 bits. The floating-point elements may not be the primary arithmetic elements, and they are unlikely to function simultaneously as in the array and signal processors. Instead, they often work in concert with a register file on multiple-step algorithms, such as square root, in addition to just add and multiply. Data rates fall from a maximum of 5 megaflops into the range of hundreds of kiloflops because of these system constraints. The simple



NAME	MNEMONIC	VALUE	EXPONENT (E)	SIGNIFICAND (S)*
NOT A NUMBER	NaN	NOT APPLICABLE	255	NOT ALL ZEROS
INFINITY	INF	$(-1)^{SIGN}$ (INFINITY)	255	ALL ZEROS
NORMALIZED NUMBER	NOR	$(-1)^{SIGN}(1.S)^{*}2^{E-127}$	1-254	ANY
DENORMALIZED NUMBER	DNOR	$(-1)^{SIGN}(0.S)^{*}2^{-126}$	0	NOT ALL ZEROS
ZERO	ZERO	$(-1)^{SIGN}$ 0.0	0	ZERO

*OFTEN CALLED F, FOR FRACTION

2. Formats. Floating-point operations and fixed-point conversions find support in the WTL 1032 and 1033 chip set. In compliance with the IEEE single-precision floating-point standard, five basic entities are defined, including special nonnumerical values.

direct controls of loading and unloading, function selection, and mode of operation on the 1032 and 1033 accommodate all of these configurations while providing near optimum performance (Table 1).

Common architecture

In the 1032 multiplier and 1033 ALU, two input operands and a single output result allow the data paths and control structure of the chips to be identical (Fig. 3). Each array is separated into three segments with nearly the same propagation time, and each segment is isolated by its own pipeline register. Furthermore, the array's function register and status are pipelined, so that these values propagate through the chip along with the associated data values.

All ports—both input and output as well as data and control—are buffered with registers on the chips. These registers, combined with three-state TTL outputs and a no-load mode of operation, ease the use of the chips in parallel bus architectures. Although the two 32-bit operands and the output result are time-multiplexed through the 16-bit ports, the clocking of input and output registers at twice the pipeline rate make this time sharing invisible. In cases where some operation is performed using a constant, bus traffic may be reduced by maintaining the constant in one of the operand registers while loading the other operand individually. Repeated multiplication or addition by a constant is a common vector operation in many high-speed applications.

Pipeline registers raise the continuous data rate through the arithmetic array logic, but at the cost of an additional clock delay for a single data value to propagate through them. This increased latency can be eliminated by using the flow-through mode in which the pipeline registers are transparent to data movement.

The status register is pipelined along with the data path so that the status at the output applies to the data concurrently at the output. The status remains constant for the two clock periods for unloading the least and most significant words of the result.

The function of the array is determined by the contents of the function register at the time the most significant words of the operands are loaded. The function is pipelined through with the data, so that it may change without all data first being unloaded from the pipeline.

Multistage ALU

The ALU provides addition and subtraction for the most useful combinations of signed and unsigned operands. Additionally, as Table 2 shows, there are the normalizing and denormalizing operations. The multiplier's only operation is multiplication, but there are four combinations of wrapped and unwrapped operands possible in its IEEE mode. The ALU array in Fig. 3 is shown in the pipeline mode with registers following each stage, all other logic being combinatorial.

Processing starts in stage ½ of the array with the loading of the most significant words of the operands. First the hidden bit is inserted by testing the exponents. If an exponent is 0, the hidden bit is a 0; otherwise, it is a 1. For two operand functions, apart from format conversions and wrapping and unwrapping, the significands must be aligned so that bits of equal weight are operated on together. This alignment begins by selecting the operand with the larger exponent. All eight of the exponent bits are compared and the result stored in a register at the start of stage 1 to indicate if operand A is larger or smaller. If only one operand is used, an appropriate constant is loaded into the B exponent register.

At the beginning of stage 1, both 33-bit operands are complete and any invalid operand for the arithmetic operation can be detected and flagged. The larger and smaller exponents are selected by multiplexers, and the smaller is subtracted from the larger. The result is the number of binary places by which the smaller operand's significand must be right-shifted for alignment with the larger operand's significand. The smaller significand is then right-shifted, while the larger is complemented if that is required by the selected arithmetic function. For single operand functions, the constant entered earlier in the smaller exponent can produce a desired shift as, for example, in conversion to integer format.

At this point, the two properly aligned significands are added and the 28-bit sum stored along with the expo-

TABLE 1: CONTROL OPERATIONS FOR WTL1032 MULTIPLIER AND WTL1033 ARITHMETIC AND LOGIC UNIT

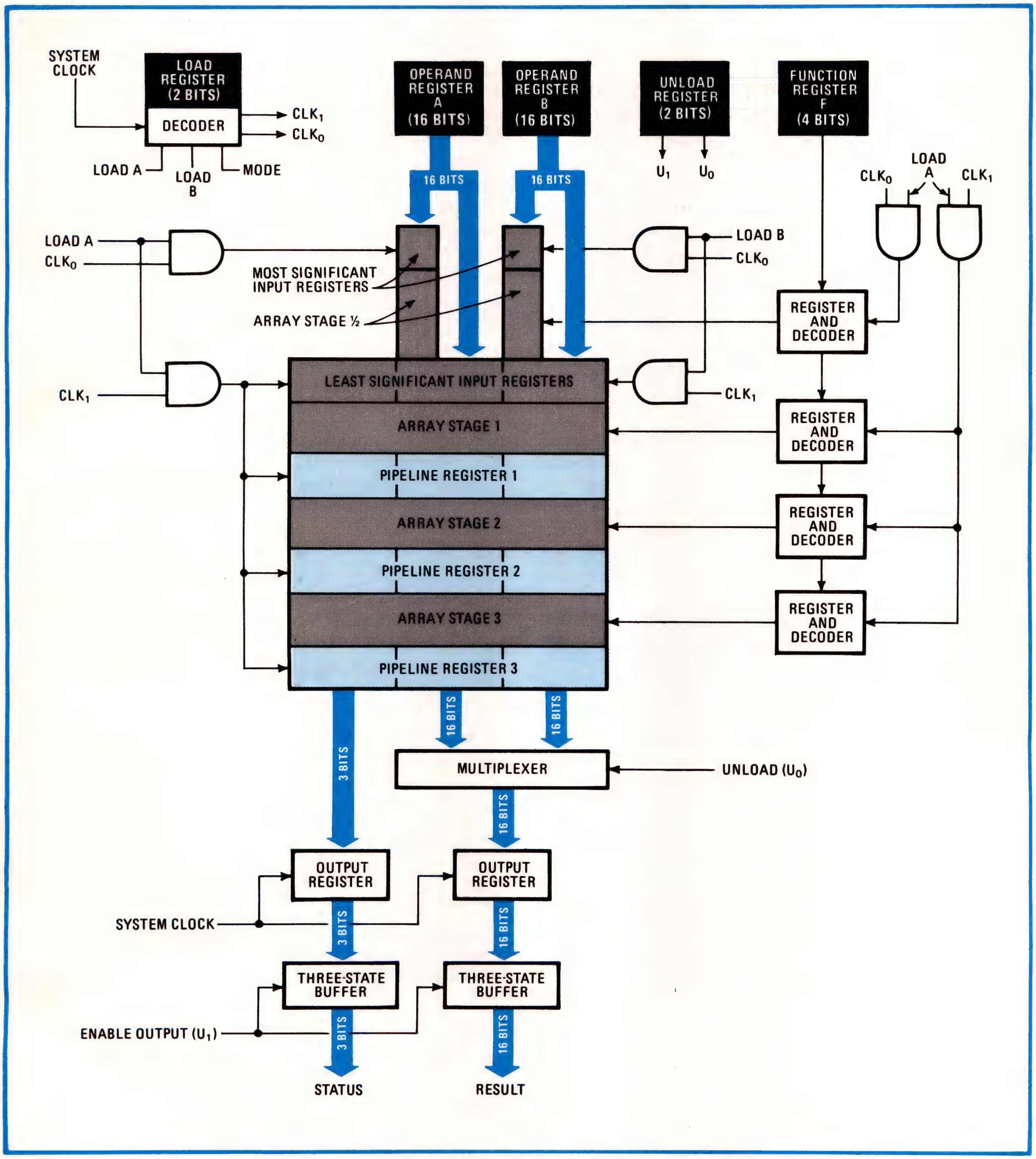
L_1	L_0	Mnemonic	Load operation
0	0	NOP	No loading
0	1	LAB	Load operands A and B into array
1	0	LA	Load operand A only into array
1	1	LMODE	Load MODE register from F and U input registers

U_1	U_0	Mnemonic	Unload operation
1	X	DAB	Disable output register's three-state outputs to high impedance state
0	X	ENB	Enables output register's three-state outputs
X	0	UMS	Unload most significant word from array into output register
X	1	ULS	Unload least significant word from array into output register

F_3	F_2	F_1	F_0	U_0	Mnemonic	Mode operation
X	X	X	X	0	FLOW	Data flows through array without pipeline registers
X	X	X	X	1	PIPE	Data is clocked through three pipeline registers in the array
X	X	0	0	X	RN	Round to nearest number, or even number if a tie
X	X	0	1	X	RZ	Round toward zero
X	X	1	0	X	RP	Round toward positive infinity
X	X	1	1	X	RM	Round toward minus infinity
X	0	X	X	X	AI	Affine infinity (sign preserved)
X	1	X	X	X	PI	Projective infinity (sign ignored)
0	X	X	X	X	IEEE	Treats denormalized operands according to IEEE standard (WTL1032 only)
1	X	X	X	X	FAST	Replaces denormalized operands with zero (WTL1032 only)

nent, sign, and status in the pipeline register at the end of stage 1. The sum is composed of 1 bit for possible overflow, the 24 bits of the format, a guard bit, an additional lower-order bit for rounding, and what is called a sticky bit. The sticky bit is the logical OR of all lower-order bits below the round bit and is used in rounding operations.

Stage 2 initially complements the sum if this is required by the combination of function choice and the sign of the sum determined in the previous stage. The resultant value in general will not be normalized at this point—that is, its most significant bit will not be set to 1. Its significand may have overflowed its original 24 bits because the two operands were of the same sign, or the value may be quite small with just a few lower-order bits set because it happened to be the



3. Single form. Both the 1032 multiplier and 1033 ALU chips use a common architecture to handle their separate functions. The shaded area is the pipelined multiplier in the 1032 and the pipelined ALU in the 1033. In the flow-through mode, the pipeline registers (color) are transparent.

difference between two nearly equal numbers.

To comply with the standard, all results must be returned normalized or at least as a denormalized number with the smallest possible exponent. The first step in the process of achieving either of these goals is to determine the location of the most significant bit that is set to a binary 1. This step is done with priority encoding logic, which returns a number equal to the displacement of the most significant bit set from the leftmost bit position.

Displacement matters

This displacement is the number of left shifts necessary to normalize the number plus the decrease in the binary exponent that must accompany the shifting to maintain the same value. The exponent is subtracted in this stage, but the displacement is stored for the more time-consuming shifting to follow in stage 3. Any underflow in the exponent as a result of decrementing generates a flag. Under this condition, the original exponent is substituted for the displacement to the shifter. This produces the shift necessary for a denormalized number, which is the desired result for a two-operand function. Under the same condition, too, the value 0 is entered for the exponent. For the wrap operation, the underflowed exponent is the desired 2's complement representation of the correct negative exponent and is retained.

With the proper amount of left shifting determined, stage 3 can complete the normalizing in its multiple-bit shifter. If the normalized 27-bit significand cannot be truncated to the 24 bits of the output format without changing its value, then it must be rounded. The sticky bit is used in this determination since it represents any exactness that has already been lost in truncation. The selected mode of rounding is accomplished with a simple adder, and the inexact result flag is set. Upward rounding of the magnitude can generate an additional higher-order bit. This, plus any previous growth, is shifted out in the rounder and the exponent incremented accordingly. Incrementing the exponent can produce overflow, which sets the exponent overflow flag.

At this point in the array, the calculation is complete, and any exceptions have been detected and flags set. The additional operations that are done at this time are for format conversions. Also, the exception flags are encoded and all output significands are reduced to 23 bits, with the most significant once again becoming hidden.

Multiplier pipes

The array of the floating-point multiplier is conceptually simpler than the ALU. Since the normalization functions are not required here (Table 3), the array's stage ½ is used only to expand the 8 exponent bits to 9, based on which of the operands have wrapped exponents, and to determine the value of the hidden bits. The expansion of the exponents makes explicit in 2's complement (and biased 127) form the negative exponent of wrapped operands.

The complete operands are loaded at the beginning of stage 1 and are tested. Denormalized operands, in addition to setting the invalid operand flag, also set the denormalized input flag signaling for their return to the ALU if operation is in the IEEE mode. Exponents are added in multiplication, and this proceeds after testing with the bias removed from one of them. Any exponent overflow or underflow values are preserved in the 10-bit sum. The sign bits of the two operands are masked off, and the output sign determined in a simple exclusive-OR operation. This relatively simple sign and exponent handling take little time compared with the multiplication of the significands.

The 24-by-24-bit significand multiplier extends across both stage 1 and stage 2. It uses an area-efficient combination of Booth encoding and carry-save adders except in the last row, which is carry-look-ahead. A full 48 bits are registered between the two stages and produced at its output. This step is necessary to maintain the 24-bit accuracy of the format, for there can be no simplification of the matrix of adders. After the final addition, however, the result is reduced to 28 bits including the sticky bit—a reduction that preserves enough precision for correct rounding, which follows in stage 3. ☐

TABLE 2: FUNCTION INSTRUCTIONS FOR THE WTL1033 FLOATING-POINT ARITHMETIC AND LOGIC UNIT

F_3	F_2	F_1	F_0	Mnemonic	Operation
0	0	0	0	WRAP A	Conversion of a denormalized A operand to one normalized with negative (wrap-around) exponent
0	0	0	1	UNWRAP A	Conversion of a normalized A operand with negative exponent to a denormalized one
0	0	1	0	FLOAT A	Conversion of 24-bit integer to 32-bit normalized floating-point number
0	0	1	1	FIX A	Conversion of 32-bit normalized floating-point to 24-bit integer
0	1	0	0	A + B	Floating-point addition of operands A minus B
0	1	0	1	A − B	Floating-point subtraction of operand A minus B
0	1	1	0	− A + B	Floating-point addition of operands minus A plus B
0	1	1	1	ABS A + ABS B	Floating-point addition of operands |A| plus |B|
1	0	0	0	A − B ABS	Absolute value of floating-point subtraction of operands A minus B
1	0	0	1	A + B ABS	Absolute value of floating-point addition of operands A plus B

TABLE 3: THE WTL1032 FLOATING-POINT MULTIPLIER

F_3	F_2	F_1	F_0	Mnemonic	Operation
0	0	0	0	A · B	Multiply normalized floating-point operands A times B
0	0	0	1	WA · B	Multiply wrapped (negative exponent) operand A times operand B
0	0	1	0	A · WB	Multiply operand A times wrapped operand B
0	0	1	1	WA · WB	Multiply wrapped operands A times B

Logic design system manages team projects

VAX-based network of graphics stations melds interactive logic design and analysis with centralized data-base management

by Ron Young, Thanasis Kalekos, and Khanh Vu, *Cadtec Corp., San Jose, Calif.*

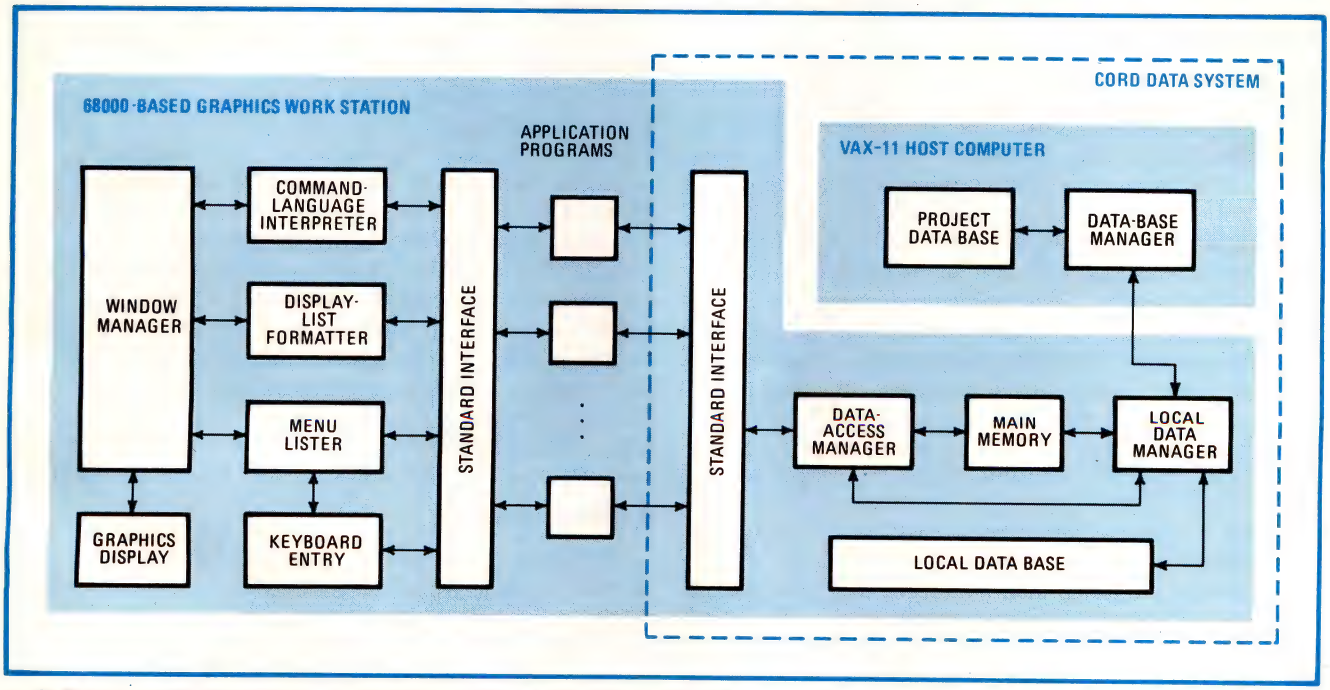
☐ The escalating complexities of electronic product development have called into existence a number of sophisticated work stations. But however well these stand-alone systems automate many logic-design tasks, they barely address the central issue of on-line circuit and system engineering: project management. Indeed, many or even most of the designs needing such sophisticated tools are huge team projects beset with a myriad administrative and logistical problems.

The series 8000 design system not only smooths and speeds schematic capture, logic analysis, timing verification, and documentation, but also squarely tackles the problems facing the manager of large team efforts in electronic design. Those problems involve partitioning a design and assigning individual tasks, cross-checking and integrating the separately developed pieces, controlling access to the project data base and managing its contents, enforcing design standards and methodologies amongst team members, and monitoring the overall progress of the design.

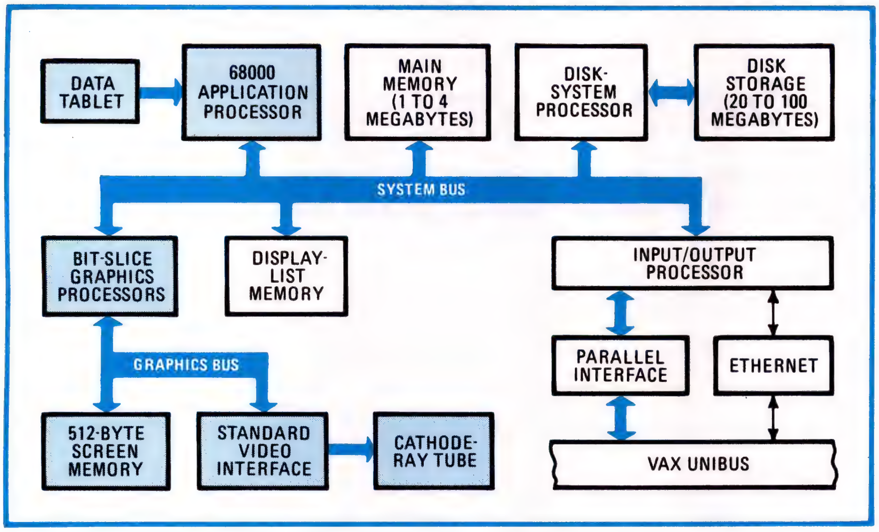
The system that solves those problems builds expressly upon a Digital Equipment Corp. VAX-11, a computer widely used in engineering and also blessed with a large base of batch-oriented computer-aided–design programs already in place. The series 8000 supplements a user's VAX with high-resolution graphics work stations and color-graphics office terminals, as well as with data-base–management software and logic design and analysis tools for interactive work.

In control

At the system's heart, the Cord data system contains and controls the consolidated data of a team of engineers contributing to a single large design (Fig. 1). Local data bases in the graphics work stations serve the individual designers on a temporary basis, holding working copies of portions of the complete base, which is stored on the VAX. Application programs for design and analysis then have access to the Cord system through a standard, object-oriented interface. Likewise, the programs have a



1. Split levels. In the Cord data system, design portions are transferred from the centralized project data base to the local base in the work station. The access manager then correlates the relational tables with user objects—the familiar gates and wires of a circuit design.



2. Local power. The model 8200 work station of the series 8000 design system runs application programs on a Motorola 68000 microprocessor. Dual bit-slice processors control the 1,024-by-1,024-pixel screen.

standard interface with user inputs entered on the keyboard or data tablet.

A multilevel scheme as in the Cord system retains the flexibility of a centralized relational data base yet offers the fast access times of a local single-user system. The centralized relational base supports the administrative controls necessary for on-line project management:

- The entire design is available at any time to any of the team members.
- Version control eliminates outdated copies of a design.
- Central storage tightens security and simplifies progress monitoring, enforcement of design standards, and archival chores.
- A standard application-independent form for data storage simplifies the incorporation of new application programs.

Data-base contents

The project data base consists of raw data in relational tables, along with object-mapping transforms—the instructions for translating from the relational formats into user objects such as gates, wires, networks, and pages. Various data types are distinguished: working copies of design portions belonging to individuals, the master copy including all revisions, documents associated with particular networks, behavioral data including simulation results and test vectors, and reference documents.

The data-base manager, also residing on the VAX, inserts and retrieves data from these tables. (It in addition allocates disk memory and administers the version-control, data-integrity, security, and archiving functions.) When requested, the manager extracts data from the project data base and transmits it to the local processor in the work station that made the request. There the local data manager enters it on a disk that now holds the local data base.

Application programs then obtain the data through the data-access manager, the program responsible for translating between user objects and the data-base formats. In this way, the user can reference and alter a data-base portion in local memory indefinitely, needing no interaction with the project data base. At the end of a session, the local data manager sends the edited portion back to the project data base, updating the relational tables to reflect all the changes. The local data base and its associated software thus act as a high-speed buffer between the user and the slow, centralized project data base.

Access to the system is controlled on a project-by-project basis, with each project possessing an independent data base. The project manager specifies which engineers are allowed access to which projects and whether that access includes authority to read, write, or delete data.

The network hierarchy established for design work also provides a natural basis for partitioning the project and assigning tasks among team members. The system permits the manager to set up individual members' assignments as attributes of any element of the network hierarchy. Read, write, and delete authority can be established on an element-by-element basis. For example, write access for a single design partition might be limited to the designer responsible for that portion, while others needing reference to it would have read-only access.

As noted before, the project data base maintains the central copy of the design for all team members. This base is further divided as the working library and the master design library. In the initial phases of design, data is stored in the working library, where team members may retrieve and edit networks according to their authority. When a given partition is completed, it is promoted to the master design library, where it is locked against write access or delete access by anyone. Only the manager or the authorized project librarian can then remove the data to the working library for some further changes.

To aid management in this process of promotion, the system incorporates an intermediate status called "pending" (see table). When ready to promote a design for viewing by the rest of the group, the designer flags his or her partition as pending. The project librarian is then notified, and team members and the librarian are allowed read-only access. After appropriate checking procedures, the manager or librarian returns the partition to the working library or promotes it to the master design library. This multilevel access scheme provides a smooth mechanism for project tracking and management.

A gracious host

The software systems of the series 8000 are designed to be transportable from one hardware environment to another. In fact, all of the programs and any user programs developed on the series 8000 may run on either the VAX (under VMS) or the 68000-based work stations (under Bell Laboratories' Unix operating system).

A key element in achieving this transportability is the use of the Mainsail language, which will allow Cadtec to take advantage of future advancements in work-station hardware without rewriting the source code. The system may be modified to run on different hardware simply by rewriting the operating-system interface. In addition to that interface, Mainsail provides memory management, a program-development language, and a library of run-time modules.

The individual work stations of the series 8000 communicate over a 10-megabit-per-second Ethernet link with the VAX. A further link to a mainframe computer supporting corporate information systems is also easily achieved through the VAX. The VAX-11 was chosen as the host processor for its good response time to many users and its large high-speed disks. At least 10 work stations can be supported without any degradation in performance.

The goal of the model 8500 office station is to extend the increased productivity of on-line design to the entire project team. A 13-inch-diagonal color-graphics terminal with 640-by-408-picture-element resolution, it embraces the many aspects of an engineer's job that do not need the power of the work station but do require access to project or design data. Documentation, communication, and minor design editing are therefore among the functions it achieves economically. The 8500 office stations tie directly to the host VAX and can make use of the Cord data system and any application programs under the VMS operating system.

The model 8200 graphics work stations, on the other hand, run application programs locally on a 68000 microprocessor (Fig. 2). A high-speed bipolar bit-slice processor (2901) controls the raster-scanned display. Hard-disk storage of 20 megabtyes may be extended to 80. Puck, data tablet, and joystick join the keyboard as standrad input devices.

The user interface

The graphics screen and data tablet constitute the primary user interface. Multiple windows may be opened on a single screen, moved about, and enlarged or shrunk as needed. The system is tutorial, minimizing the formal training required. A context-oriented help function provides guidance and explains errors.

The system also maintains a user profile on each engineer for his or her convenience. This file may tailor the display and applications to individual preferences, keep track of what project was last worked on and when, automatically return to the last referenced design step, and control access to project data.

Like other menu-driven interfaces, system functions may be selected with a single command. Furthermore, menus are also used in a graphics-assisted command language to build command lists for producing schematics and tests. A command list is a series of commands that are executed when the list is invoked, saving typing time and automatically forming the correct syntax. As a result, the engineer can focus on problem solving instead of wrestling with an awkward development system. This feature is particularly handy during simulations where the same series of commands might be used many times with different variables.

Likewise, all commands issued to the system are recorded so that recovery procedures can be readily implemented following a system failure. The command logs can also be edited and re-used as input lists, avoiding repitition of lengthy sequences. Also, an undo command will backtrack one step after a mistaken command.

Logic design and analysis

Application programs available at present cover schematic entry, logic simulation, timing analysis, behavioral analysis, documentation, and test-tape generation. Other tools for logic design and development are planned.

Hierarchical schematic entry is controlled with the puck and data tablet. A library of standard Institute of Electrical and Electronics Engineers' symbols for logic design is maintained on the system. Users may create, store, and add to the menus other symbols using graphical editing commands.

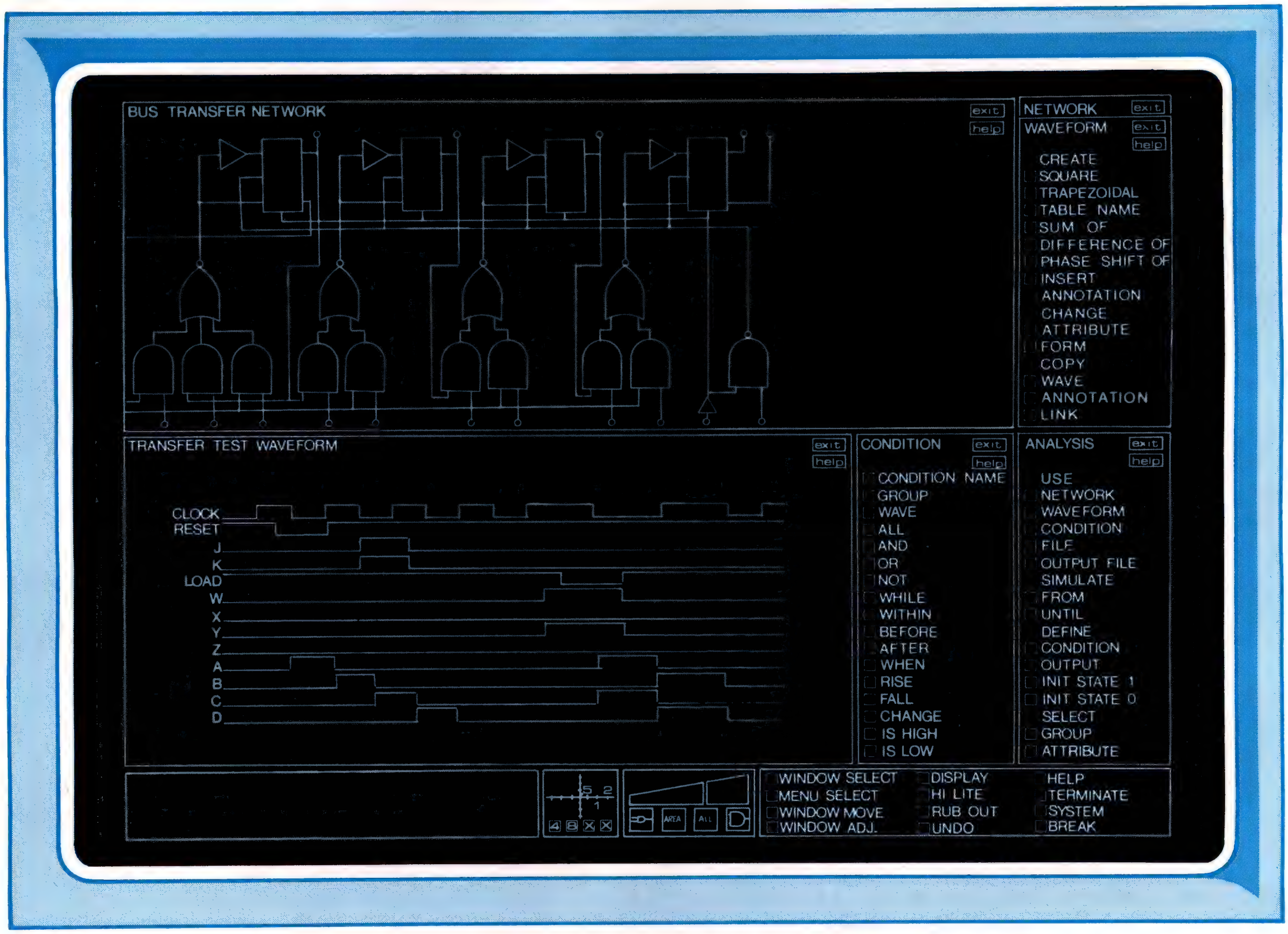
Each network is treated as a "design space," an arbitrarily large collection of elements. Consequently, users face no restrictions on page size. With such virtual paging, boundaries of physical pages for plotting can be set or changed at any time. A hierarchy of these networks of any size can be created in any fashion, from the top down, bottom up, or some mix of both.

Multiple views of any network can be shown at the same time—that is, any of several levels of detail may be selected at will in each portion of a network. Also, different implementations of the same function can be created, stored, and compared in tests. Each version can carry as attributes information about the function, its elements, signal values, design rules, and so on. Such attributes are then available as parameters for any of the applications programs.

Extensive checking procedures run constantly to ensure that a design follows the rules for the particular technology employed. Two types of checking are performed: automatic checks flag unconnected networks, pads, or terminals and mismatched network names and bus widths, while user-specified checks look at fan-in and

NETWORK STATUS CONTROL IN SERIES 8000 DESIGN SYSTEM

Network status	Access controller	Design access	Notification of changes	Tracking facilities
Working	owner	read/write (owner only)	none	command log, version control
Pending	librarian	read only	all team members	results of checking
Promoted	librarian/manager	read only	all team members	usage of promoted designs



3. Virtual analyzer. Stimulus waveforms created with the menu at upper right are applied to a logic design such as the bus transfer network shown. Outputs can be monitored and relevant circuit sections highlighted.

fan-out, delay limits, drive power requirements and capabilities, and capacitive loading. A "design alert" is issued whenever a design fails a rules check.

To eliminate the possibility of mismatched interfaces between separately designed portions, explicit provision is made for the definition of an interface specification. Each designer can automatically check his portion of the design against the interface specification for adjoining portions during the design process. The order and number of pins, network names, and technology constraints are thus guaranteed to be consistent across any number of partitions.

Simulation capabilities of the series 8000 are combined with behavioral analysis to provide the software equivalent of a logic analyzer. Network design on the system automatically produces output formatted for either Cils or Tegas 5 simulators. The former is Cadtec's nine-state interactive logic simulator; the latter is supplied by Comsat General Integrated Systems of Austin, Texas.

Simulation inputs and outputs can both be viewed as waveforms, using the waveform editor and behavior analysis programs, respectively. Figure 3 shows a waveform analysis screen with a set of waveforms that is being used to test the bus-transfer logic shown in the upper window. The engineer defines the waveforms, runs the simulation program, and views the results. Portions of a circuit affected by particular stimuli may be highlighted, as may waveforms corresponding to particular nodes.

Furthermore, waveforms can be searched in time for the occurrence of particular conditions, such as a given bus address. Using an English-like condition language, elements of the logic schematic can be located and highlighted on the basis of the occurrence of specified conditions. The condition-language commands are entered from a menu and in consequence do not require a special syntax to be learned. The language additionally lets the designer make assertions about the behavior of the design that will be automatically checked against the simulation results.

Several output modes are available for interfacing to external programs. The network listing that serves as input to Tegas can also provide input to gate-array or standard-cell manufacturers and for checking circuits extracted from physical layouts. Test vector outputs are compatible with the formats for the Sentry VII testers of Fairchild.

In addition, the Cadtec Design Interchange Format constitutes a high-level, humanly readable design language that can embrace an entire design description, including all elements and their attributes and connectivity. A CDIF file may be used to transport a complete design from one system to another or for transferring the output of external simulators and rule checkers into the Cadtec system for analysis and documentation. ☐

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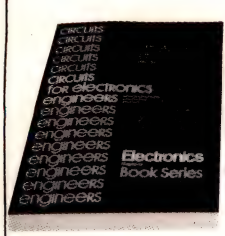

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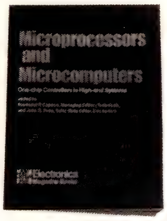

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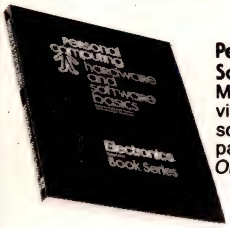

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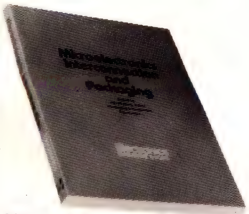

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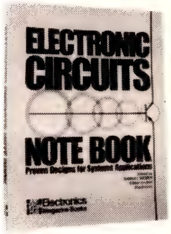

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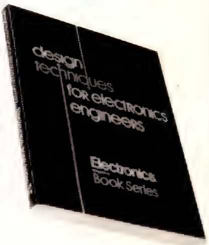

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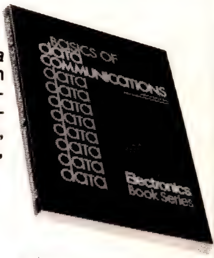

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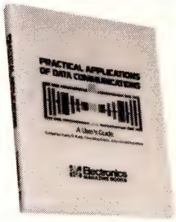

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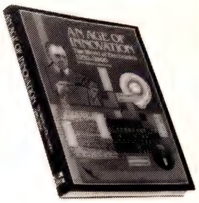

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Scanned electron-beam probe shows surface acoustic waves in action

Strobed beam produces real-time images on a TV-like display of the activity on the surface of SAW delay lines, filters, and convolvers

by Hans-Peter Feuerbaum, Ulrich Knauer, Hans-Peter Grassl, and Richard Veith

Siemens Central Research and Development, Munich, West Germany

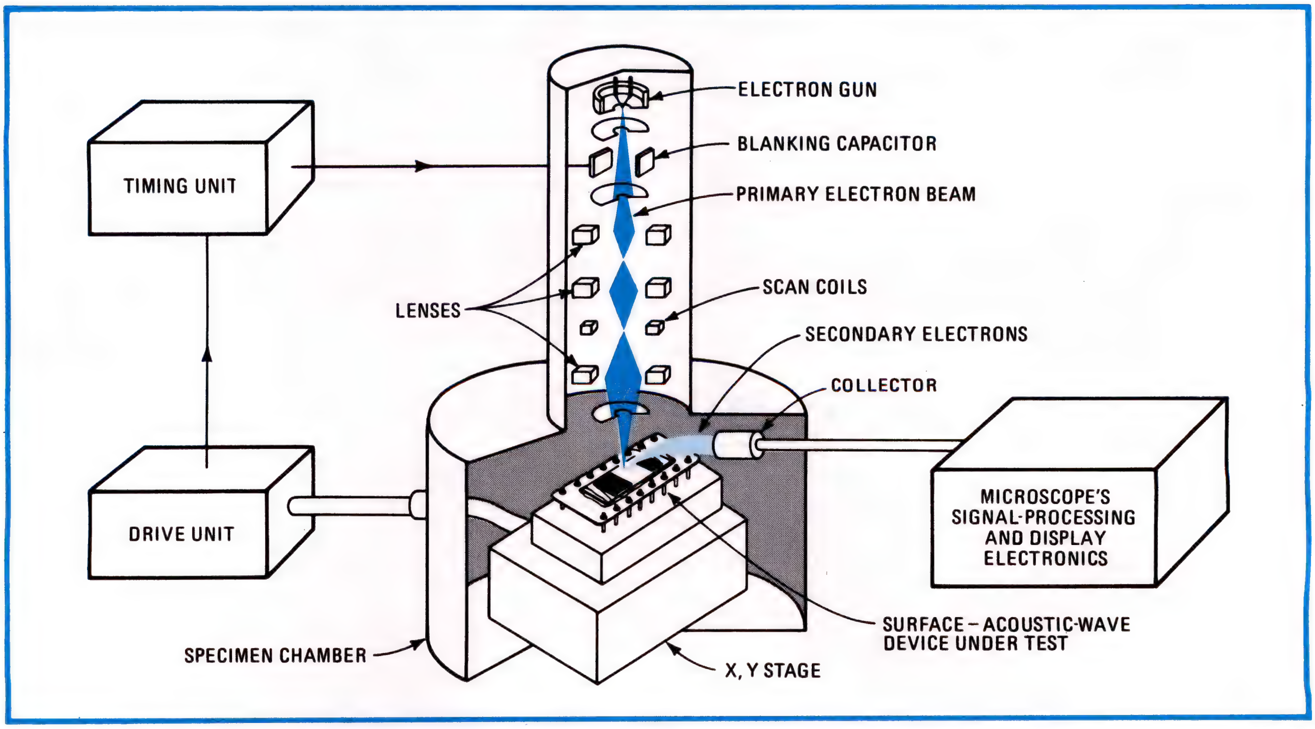
☐ In no electronic system can an optimum signal-to-noise ratio be achieved without filters that exactly match a signal's spectrum. And no technique offers better solutions to this problem than does signal processing based on surface acoustic waves.

But to fully exploit the potential of SAW technology (see "Making surface acoustic waves," opposite), such secondary effects as the diffraction, refraction, and reflection of surface acoustic waves or the generation of bulk acoustic waves must be incorporated into the design models. The necessary knowledge about these secondary effects can be obtained by imaging these waves, and capacitive and laser probes have been used to this end. However, these methods employ tedious point-by-point measurements, and it may take several hours to map the acoustic field radiating from a transducer.

In contrast to these time-consuming approaches, a scanning–electron-beam microscope, or SEM, operating in a stroboscopic voltage-contrast mode, can supply real-time images of acoustic waves as they propagate across the surface of a piezoelectric crystal. Drawing on experience with the electron-beam probing of integrated circuits [*Electronics,* July 14, 1981, p. 105], Siemens engineers set up an apparatus that produces such images on a screen at TV scan rates, with the result that the activity of SAW devices can now be seen "live" in a TV- or movie-like presentation.

Probing microscope

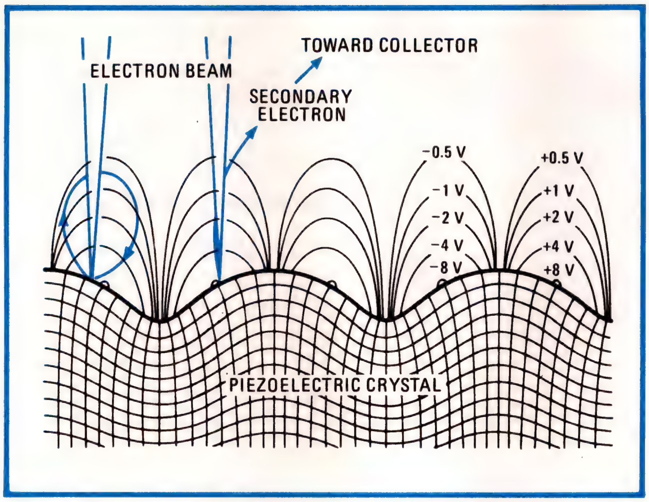
For electron-beam probing, a SAW device is mounted in the specimen chamber of an SEM and an rf signal applied to its input transducer through a drive unit (Fig. 1). In the column of the microscope, an electron beam is generated by the electron gun, focused by a magnetic lens system, and scanned by deflection coils across the surface of the device. Low-energy secondary electrons



1. Displayed. If a surface–acoustic-wave device is put under an electron microscope and has a focused electron beam scanned across it while it is in operation, the resulting secondary electrons can be collected and displayed on a cathode-ray tube in real time.

released from the surface are extracted by a collector tied to a high positive voltage. After amplification, the secondary electrons' signal is displayed on a cathode-ray tube, revealing the topography of the device.

For stroboscopic investigations at the high frequencies typical of signal processing, the SEM is equipped with a timing unit and an electrostatic beam-blanking system capable of pulsing the electron beam with a minimum pulse width of 350 picoseconds. The duty cycle, typically 10%, is kept constant by the timing unit at a rate that is independent of the pulse repetition rate. The narrow duty cycle and the high electron-beam current (an unpulsed 10^{-8} ampere) make for an almost noise-free stroboscopic display on a TV monitor.



2. Voltage contrast. The trajectories of secondary electrons are influenced by the local electric fields that accompany surface acoustic waves. Regions with a positive potential appear dark in the resulting image, while regions with a negative potential appear bright.

Minimum charge

The SEM's electron optical column is optimized in the low acceleration-voltage range of 1 to 3 kilovolts. Consequently, an acceleration voltage may be chosen that equalizes the currents of the back-scattered and secondary electrons flowing against the electron-beam current. This minimizes charging of the insulating crystal surface.

In scanning electron microscopy, several methods are possible for the imaging and measurement of surface acoustic waves. Each utilizes the electric fields set up by crystal-lattice deformations provoked by a surface acoustic wave. These fields retard the trajectories of the secondary electrons emitted from regions with positive voltages and so force most of them back to the surface of the SAW device. In contrast, secondary electrons from regions with a negative voltage see an extraction field that speeds them up on their way to the collector (Fig. 2). This modulation of the secondary-electron current by local electrical fields can be displayed as an image on a CRT in a voltage-contrast mode.

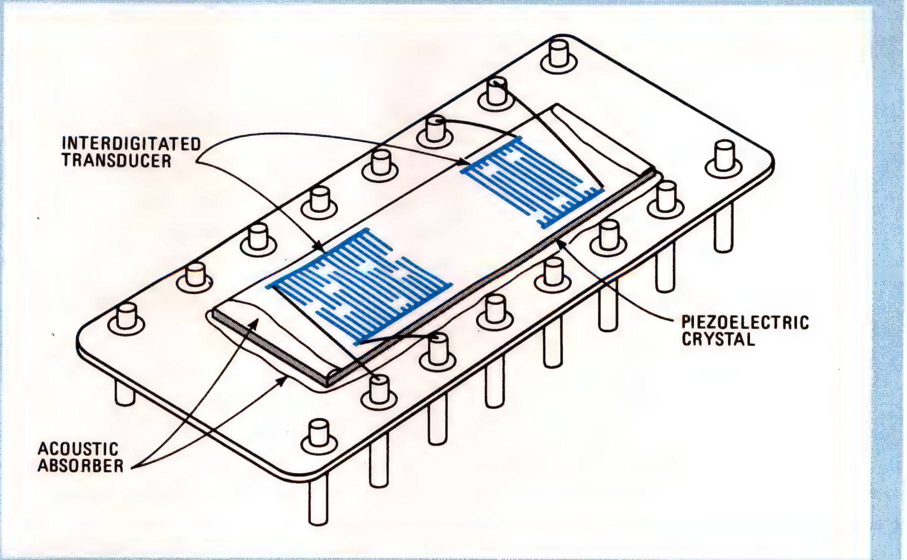
To image high-frequency fields of traveling surface waves, however, stroboscopic voltage contrast has to be used. In this mode, the electron beam is pulsed synchronously with the wave excitation by a fast beam-blanking system with the 10% duty cycle already mentioned. Now the electron beam strikes the SAW device only at a certain phase (Fig. 3).

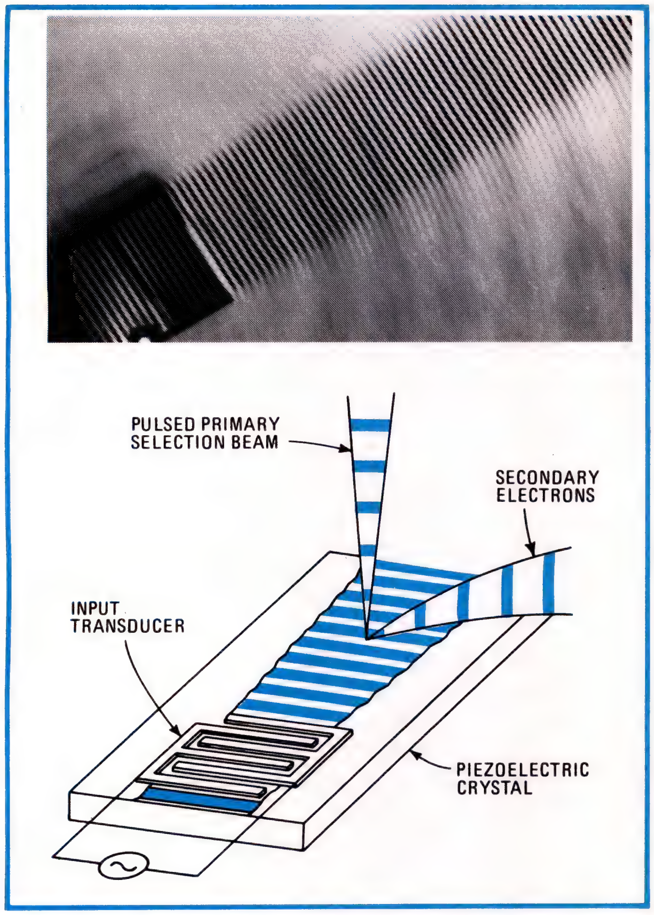
The resulting pulse-like signal of the secondary electrons is smoothed and reveals the traveling-wave pattern. Figure 3 also shows the image of waves generated by a

Making surface acoustic waves

To generate surface acoustic waves, an rf signal is applied to the electrodes of an interdigitated transducer on the surface of a piezoelectric quartz or lithium niobate crystal, as shown in the figure. State-of-the-art microlithography makes it possible to vary the position and overlap of the transducer fingers in steps of 0.01 micrometer within a field of 10 by 10 millimeters. With such an arrangement, both the amplitude and the phase of the SAW device can be adjusted to a resolution of 10^{-6}.

Furthermore, through the controlled, mutual interference of the waves generated at each transducer finger, the frequency response of a SAW transducer can also be tailored to almost any desired shape. Finally, computer-aided design methods based on models of the generation and propagation of these waves are used to configure SAW devices such as resonators, delay lines, bandpass filters, correlators and convolvers operating in the 10-to-1,000-megahertz range.

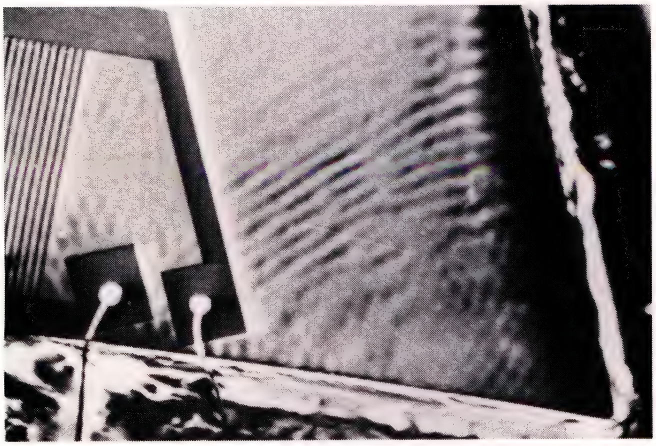




3. Strobed electron beam. If the scanning electron beam is pulsed synchronously with the wave excitation of a SAW device, the result is a stationary image of the traveling surface acoustic waves radiating from a transducer on the device's lithium niobate substrate.

transducer at 36 megahertz. The details of this wave propagation can be studied by using the wave-packet mode. Here, the emitting transducer is excited by a sinusoidal signal that is interrupted after several periods.

To display the wave packets thus propagated, the electron beam is pulsed synchronously with the repetition rate of the wave packet and with a duty cycle of about 0.1%. This results in a wave packet whose propagation can be studied without interference in it caused by other waves. Figure 4 shows the reflection of waves from a crystal edge that is not covered by an acoustic absorber; the reflection is displayed in the wave-packet mode.



4. Reflected. If the emitting transducer is excited by a sinusoidal signal that is interrupted after several periods, surface waves may be studied in packets. The reflection of a packet of waves from a crystal edge not covered by an acoustic absorber is shown in this view.

Measuring amplitude

But though stroboscopic voltage contrast shows wave propagation in detail, it allows only a rough estimation of wave amplitude. Yet a quantitative analysis of amplitude is mandatory for verifying design models.

To accomplish this, a special setup (Fig. 5) was developed to operate in the stroboscopic voltage-contrast mode with a constant beat frequency. This is obtained by setting the operating frequency of the beam blanking several kilohertz away from that of the SAW device. The electron beam then "sees" traveling waves propagating with the beat frequency.

The alternating signal of the secondary electrons is measured in a lock-in amplifier and kept constant by a feedback loop that controls the amplitude of the voltage across the input transducer by means of a p-i-n modulator. The control voltage applied to the p-i-n modulator is a measure of the local wave amplitude.

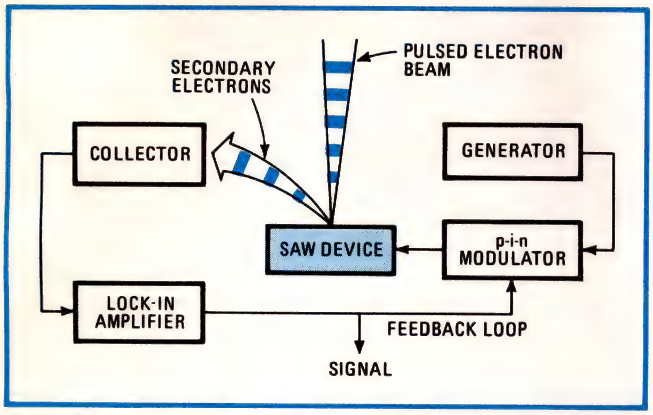
For every SEM measurement, a knowledge of the interaction between the electron-beam probe and the device is of primary importance. This interaction is due to the fact that a pulsed electron beam can release energy in various forms that can in turn generate acoustic waves. Consequently, because the pulsed beam is itself a point source of surface and bulk waves, these signals might falsify the results of probing. This effect was investigated by plating a transducer on a crystal surface and using it to detect waves generated in another part of the crystal by the electron beam. The amplitude of these waves turned out to be immaterial, being several orders of magnitude less than the minimum SAW amplitude resolved by stroboscopic voltage contrast.

The methodology of electron-beam probing has already been applied to identify a number of second-order effects in SAW signal-processing devices. Incorporating these effects into more sophisticated design models and minimizing them by an appropriate transducer layout has substantially improved the performance of SAW devices.

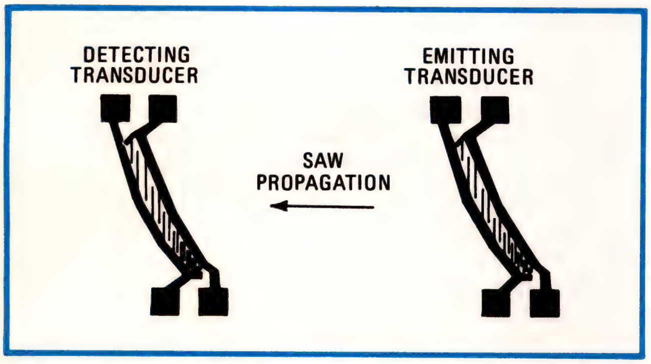
Delayed by a line

The simplest form of SAW signal processing is as a time delay. SAWs propagate at about 3,300 meters per second, which is the equivalent of a 3-microsecond delay per centimeter, five orders of magnitude slower than electromagnetic waves. Figure 6 shows the layout of a delay line on lithium niobate. Finger width and spacing are made to decrease continuously from the top to the bottom of the transducer in order to obtain a large bandwidth. Additionally, the transducers are slanted to provide different propagation paths for each frequency within the passband.

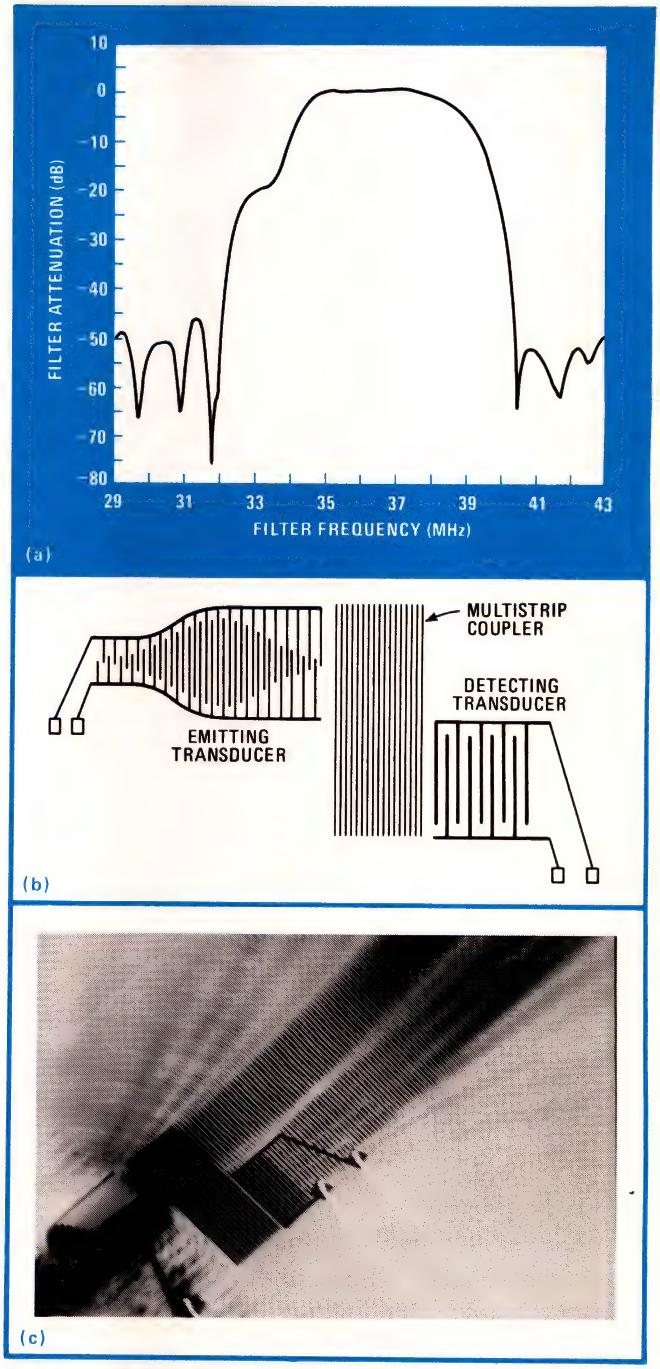
Waves at a particular frequency are radiated only from that region of the transducer where the acoustic wavelength matches the finger period. The narrow SAW beam interacts with just a few fingers. Variations of acoustic



5. Amplitude measurement. A feedback loop controls the voltage across the emitting transducer of the surface-acoustic-wave device, so that a constant secondary-electron signal is produced. The control voltage then is a measure of the local wave amplitude.



6. Delay. This broadband SAW delay line has a time delay of up to 20 μs. Transducers are slanted to provide different propagation paths for each frequency. A strobed electron micrograph would display surface acoustic waves radiating from the delay line at 300 MHz.



7. Intermediate frequency. The frequency response of a SAW i-f filter (a) for a television application can be realized with the surface-acoustic-wave filter of (b). The micrographs show surface waves radiating from the input transducer at 36 MHz (c).

power with frequency as well as SAW reflections from the transducers are thus minimized. By this means, a frequency response centered at 240 MHz, a bandwidth of 120 MHz, ripple of less than ±0.1 decibel, and more than 55-dB spurious-signal suppression were achieved for time delays as long as 20 μs.

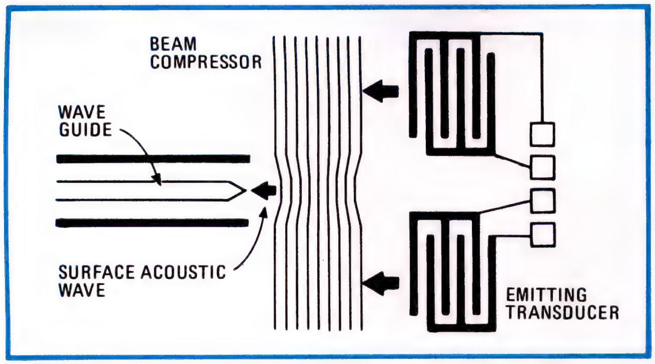
A SAW filter

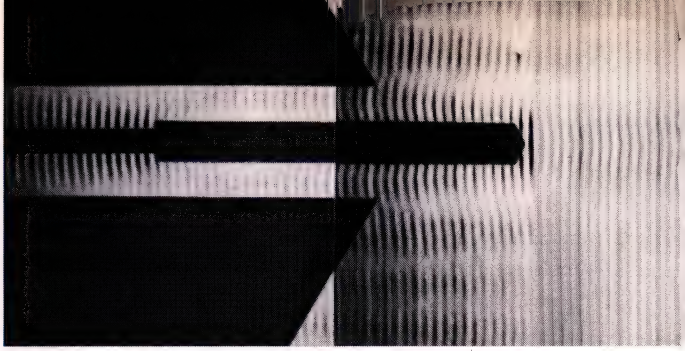
SAW transducers generally have bandpass characteristics. Within this limit, their frequency responses can be tailored to almost any shape. One particularly complex example is the intermediate-frequency filter in TV receivers (Fig. 7). This filter has a twofold function, to shape the spectra of picture, color, and sound signals and to reject adjacent-channel signals. The SAW implementation of this filter consists of a weighted input transducer designed for the desired frequency response, an output transducer, and a multistrip coupler; the last element piezoelectrically couples surface waves to an adjacent track but lets unwanted bulk waves propagate straight on past the output transducer.

At the center frequency of 36 MHz, part of the SAW power is coupled to the output transducer. At the neighboring channel's sound-carrier frequency of 40.4 MHz, of which a high rejection is required, the input transducer still radiates acoustic power but a 180° phase shift occurs within the SAW beam, so that the multistrip coupler does not couple SAW power to the output transducer.

Spurious bulk waves can be seen to be radiated in a direction perpendicular to SAW propagation, but these waves do not reach the output transducer and do not affect the filter's response.

SAWs do not propagate with rectilinear wavefronts. SAW wavefronts are distorted by diffraction. This becomes particularly severe for devices that have to be fabricated on small chips, where SAW diffraction may limit the stopband rejection to less than 35 dB. However,





8. Convolved. Two waveforms counterpropagate in a SAW delay line and are convolved by nonlinear mixing. To enhance acoustic power density, surface waves are compressed by a multistrip beam compressor into a narrow beam and fed into a waveguide.

if SAW diffraction is accurately modeled, the design can compensate for it, and a stopband rejection of more than 45 dB can be achieved even on small chips.

Surface acoustic waves are capable of even more complex signal processing, such as the convolution of broadband signals. Processing signals with a 100-MHz bandwidth and 10-μs duration, SAW convolvers carry out the equivalent of 10^{11} multiplications per second and are among the fastest signal processors available.

A SAW convolver consists of a delay line on a lithium niobate substrate with two input transducers and one output electrode along the delay path (Fig. 8). If one signal is fed to one transducer and another signal to the other, the two signals counterpropagate in the delay line and are multiplied locally because of nonlinear mixing in the substrate. The spatially integrating output electrode then supplies a signal that is the convolution of the two input signals time-compressed by a factor of two.

Because of the weak nature of the nonlinearity, the acoustic power has to be concentrated if the SAW is to be efficient. Surface acoustic waves generated by wide-aperture input transducers are therefore compressed by a multistrip beam compressor into a narrow beam and are then fed into a wave guide formed by the output electrode and typically five wavelengths wide.

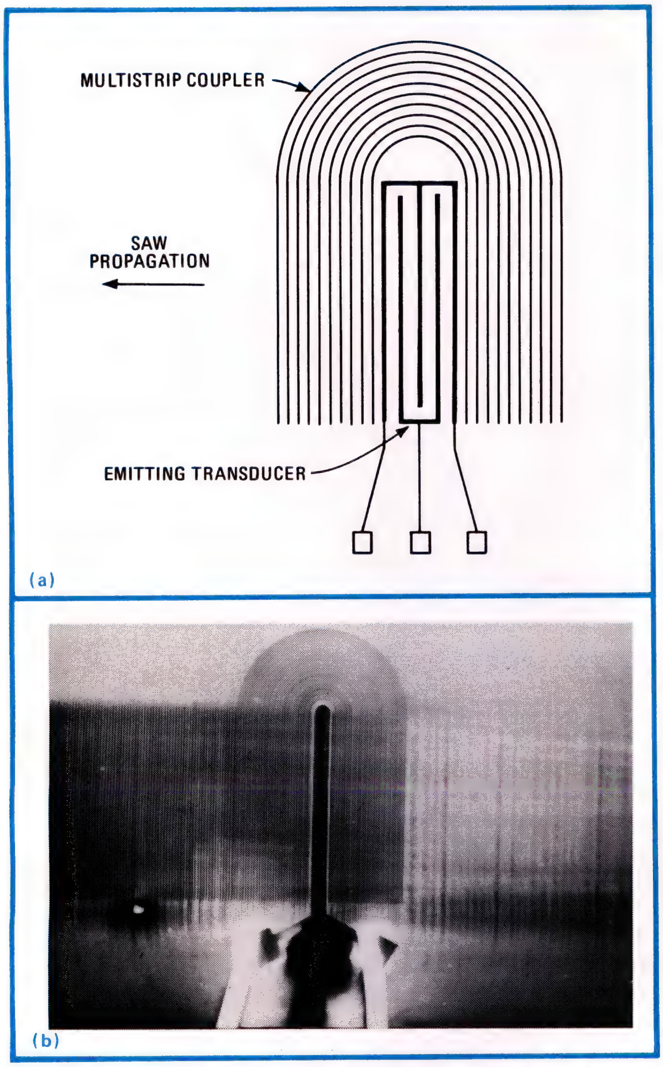
In an early device, antisymmetric wave-guide modes were found to produce spurious signals. Examination with an SEM proved that these modes were excited because of the asymmetric design of the beam compressor. Antisymmetric modes were eliminated by using a beam compressor redesigned to be perfectly symmetric.

Achieving unidirectionality

In the previous examples, 3 dB of acoustic power were lost at each transducer because surface acoustic waves are radiated in two directions. Unfortunately, the better a bidirectional transducer is matched to its load, the more it tends to reflect acoustic waves. To reduce reflections, bidirectional transducers must be deliberately mismatched, and mismatch accounts for most of the 15-to-35-dB insertion loss typical for SAW components.

One method of preventing these losses is to arrange a U-shaped multistrip coupler around the transducer. If the transducer is placed 1/8 wavelength apart from the center of the coupler, waves add up constructively in one direction and destructively in the other, and the transducer becomes unidirectional. If unidirectional transducers are matched to an electric load, insertion loss as well as reflections are reduced.

When the SEM examines such an arrangement, it is seen that SAW radiation is more intense towards the left than towards the right (Fig. 9). Unidirectionality is not perfect because of spurious waves radiated in the lower region of the interdigitated electrodes and in the upper part of the multistrip coupler. These spurious waves must be suppressed in order to improve the directivity of the arrangement. ☐



9. Unidirectional. A U-shaped multistrip coupler (a) is employed to cancel waves radiated toward the right and to enhance those radiated to the left (b). With this arrangement, insertion loss is reduced, and so, too, are reflections of surface acoustic waves.

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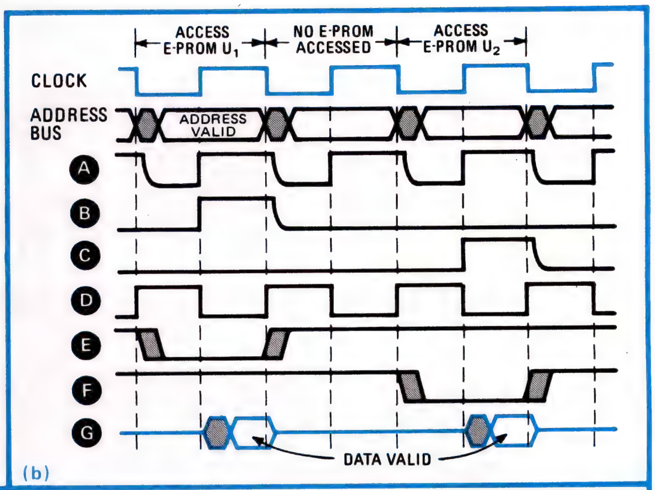
Strobing limits power needed by E-PROMs

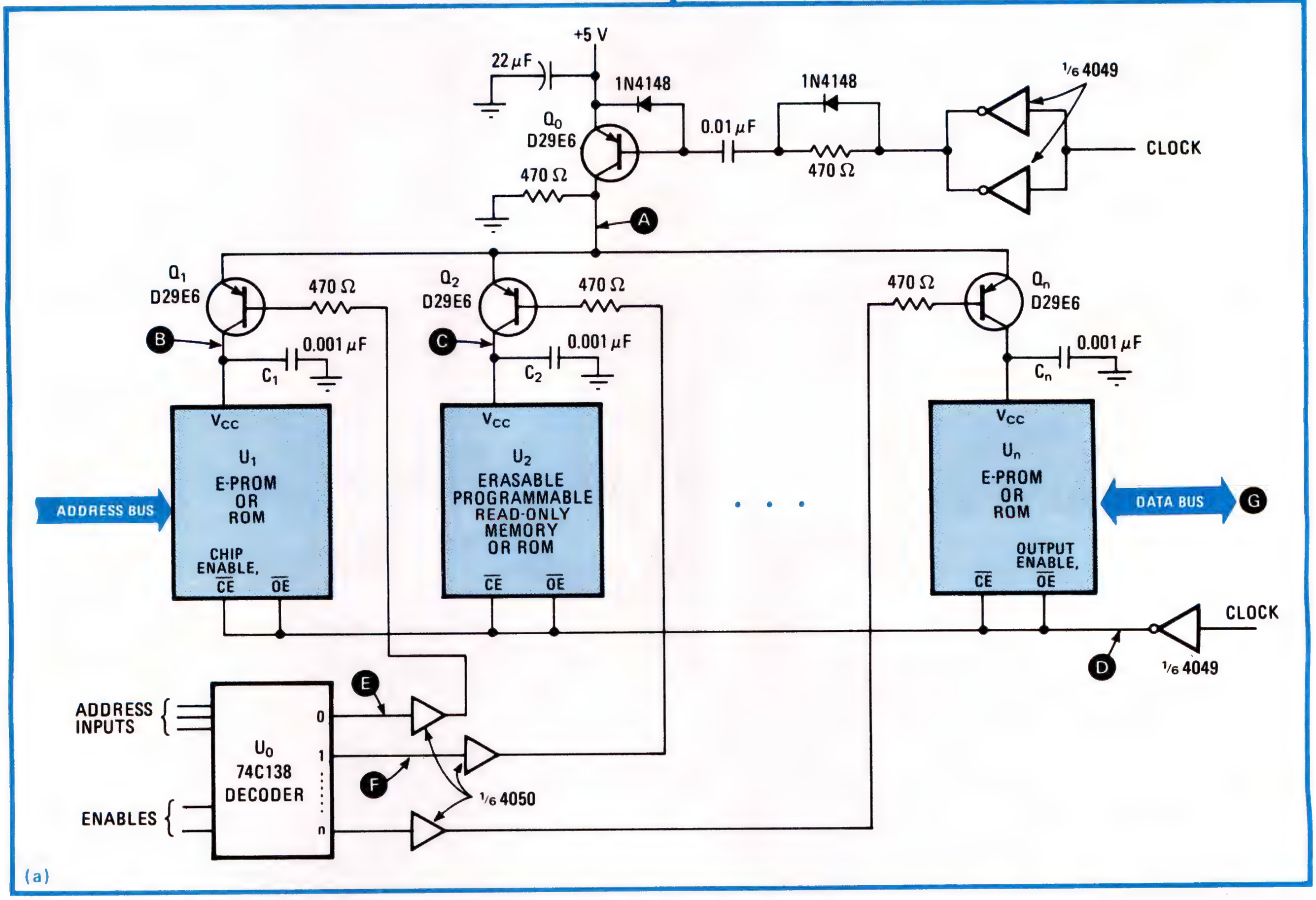
by Don Schuman
Redmond, Wash.

Engineers faced with the problem of reducing power consumption in systems employing erasable programmable read-only memories can now turn to this strobing circuit (a). It activates only the E-PROM that is accessed during any clock cycle. Hence the amount of power saved is proportional to the number of E-PROMs used in the system and their relative access times.

Transistor Q_0 controls the +5-volt supply's on-off timing, which is set by the input clock pulse after its passage through some associated circuitry, and transistors Q_1 through Q_n determine which E-PROM must be powered by the +5-V pulse supplied by Q_0. The address-decode logic, produced by decoder 74C138, controls the conduction of transistors Q_1 through Q_n. In addition, capacitors C_1 through C_n stabilize supply V_{cc} and stop oscillations by damping the undesired frequencies.

The timing requirements (b) indicate that the chip-enable and output-enable signals must be high for at least 50 nanoseconds before V_{cc} falls below 4.75 V. This technique is designed to work with type 2716, 2516, 2732, 2532, 2764, and 27128 E-PROMs. ☐





Conserving energy. By strobing only the particular erasable programmable ROM that is accessed during any one clock cycle, the design (a) lowers power requirements for a system that uses a number of E-PROM or ROM devices. The timing diagram (b) shows the relationship between the access time for each E-PROM and the clock cycle.

Voltage-pulse converter needs no supply regulation

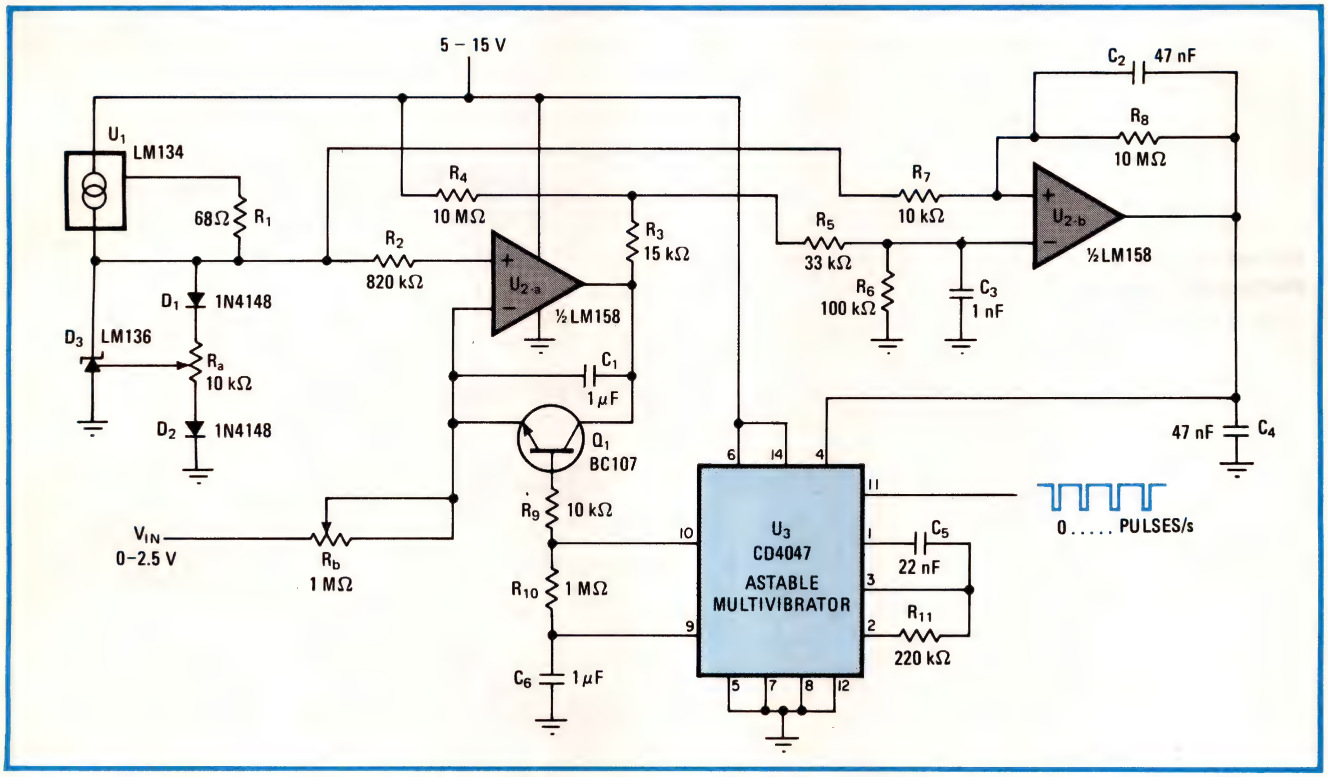
by F. Ypenburg
CSIR, National Physical Research Laboratory, Pretoria, South Africa

Suitable for low-frequency applications, this voltage–to–pulse-train converter consumes little power and is relatively insensitive to power-supply variations. For a variation between 5 and 15 volts dc, the circuit yields an accuracy of better than ±0.5%. The design has no need of a regulated supply and is attractive for battery-powered applications.

The current through potentiometer R_b charges capacitor C_1, which in turn determines the rate of the output pulse. For an input voltage of 2.5 V, this current and consequently the output pulse rate is zero, while for $V_{in} = 0$ V, the rate is 5 pulses per second and the current is 1.8 milliamperes.

When the output voltage of operational amplifier $U_{2\text{-a}}$ reaches 3.3 V, comparator $U_{2\text{-b}}$ changes state and triggers gated astable multivibrator U_3. This action sends a pulse to resistor R_9, which starts transistor Q_1. As a result, C_1 discharges through Q_1, and R_{10} charges C_6. Therefore, when C_6 reaches half the supply voltage, it resets the multivibrator and the cycle starts again.

The 2.49-V reference for comparator $U_{2\text{-b}}$ and the starting voltage for C_1 are generated by the network comprising current source U_1, potentiometer R_a, and diodes D_1 through D_3. In addition, R_7 and R_8 stabilize the comparator through hysteresis while C_2 allows it when necessary to remain in low state for a longer period of time. ☐



Converter. This voltage–to–pulse-train converter provides a pulse-rate output that is insensitive to power-supply variations and is suitable for low-frequency applications. The circuit consumes 1.8 mA and is accurate to within 0.5% for a supply variation between 5 and 15 V dc. For an input voltage V_{in} ranging from 0 to 2.5 V, the output pulse rate is between 5 and 0 pulses per second.

Jump-on-reset helps iSBC-80/20 use its RAM fully

by D. M. Brockman and L. A. Malchodi
Boeing Airplane Co., Seattle, Wash.

It is often desirable for a microcomputer to be able to set the address of its random-access memory initially at zero. That ability is conferred on Intel's iSBC-80/20 by this jump-on-reset circuit. The microcomputer is thereby enabled to run a CP/M-compatible operating system. In addition, the circuit provides a vector control for the programmable read-only memory at address $0F800_{16}$ and allows the monitor program to load the operating system in the lower address space of the RAM. The on-board PROM may be disabled by installing a jumper from pad $W_{2\text{-a}}$ to $W_{3\text{-a}}$.

Once a reset command is issued, the INIT signal from the Multibus sets the gate latch comprising NAND gates $U_{1\text{-a}}$ and $U_{1\text{-b}}$. This latch enables bus driver U_4 and disables the RAM with the INH1 pulse. With the address

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```
A i D                                                             02
Input-                                                           /83
PID - CONTROLLER INITIAL DESIGN

+-----------------------------------------------------------------+
!                                                                 !
= controller:                                                     !
! prc;                                                            !
!                                                                 !
+-- FOR ----------------------------------------------------------+
!                                                                 !
! channel system = 0 to 9;                                        !
!                                                                 !
!        +-- DO --------------------------------------------------+
!        !                                                        !
!        ! get analog values and verify;                          !
!        !                                                        !
!        ! compute controller output ( PID - algorithm);          !
!        !                                                        !
!        +-- IF --------------------------------------------------+
!        !                                                        !
!        ! controller output positive                             !
!        !                                                        !
!        +-- THEN ---------------------------+-- ELSE ------------+
!        !                                   !                    !
!        ! turn on heating;                  ! turn on cooling;   !
!        ! attention!!!! check power         !                    !
!        ! consumption;                      !                    !
!        !                                   !                    !
!        +-- IF -----------------------------+                    !
!        !                                   !                    !
!        ! power consumption too high        !                    !
!        !                                   !                    !
!        +-- THEN ----------------+-- ELSE --+                    !
!        !                       !           !                    !
!        ! release alarm;        !           !                    !
!        !                       !           !                    !
!        +-- IFEND --------------+-----------+                    !
!        !                                   !                    !
!        +-- IFEND --------------------------+--------------------+
!        !                                                        !
+--------+-- DOEND -----------------------------------------------+
!                                                                 !
! end controller;                                                 !
!                                                                 !
+-----------------------------------------------------------------+
```

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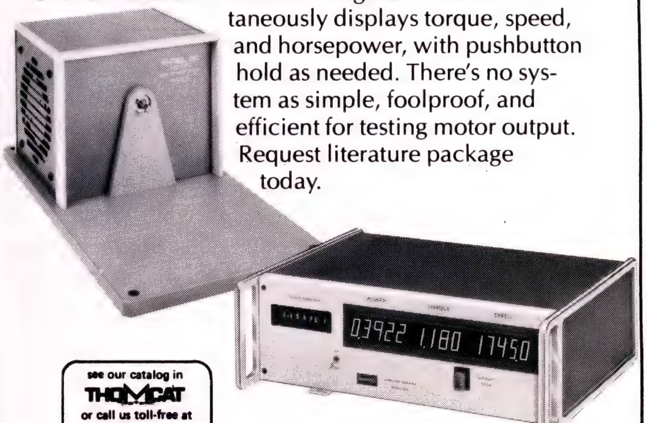

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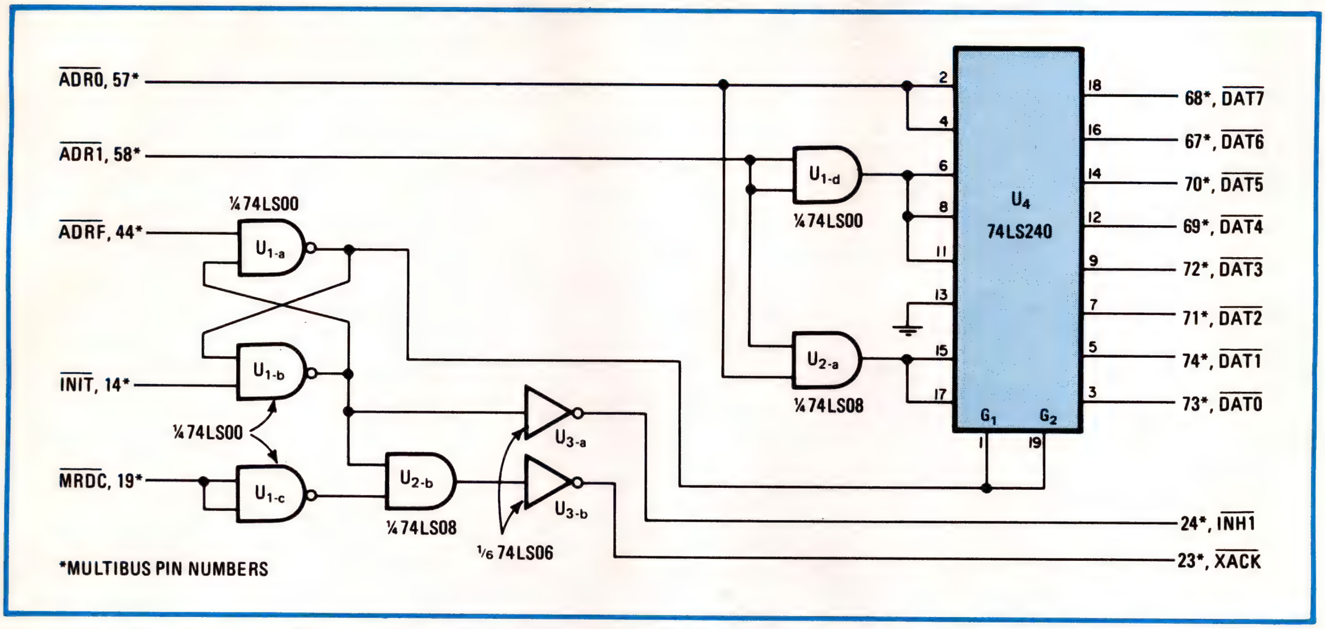


Jump. Using a few logic gates, this jump-on-reset circuit allows Intel's iSBC-80/20 microcomputer to operate with its random-access memory initially set at address 0. After the processor is reset, the circuit also provides the monitor PROM with a vector to the $0F800_{16}$ address.

bits set at 0, the operand code $0C3_{16}$ for JMP is enabled on the bus and fetched by the central processing unit. Gates U_{1-c}, U_{2-b}, and U_{3-b} generate signal XACK, which enables the central processing unit to fetch the op codes sent on the bus.

When JMP is decoded, the CPU fetches the low byte of the jump operand from address 1 and the high byte from address 2. As a result, the output of gate U_{2-a} is low, and a 0 is sent on the bus. But for address 2, the output of U_{1-d} is high and address $0F800_{16}$ is transmitted. This condition forces the CPU to execute a jump.

When the CPU fetches the next byte from the new address space, the most significant byte of the address bus, ADRF, is set and the gate latch is reset, making the circuit inactive. ☐

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay \$75 for each item published.

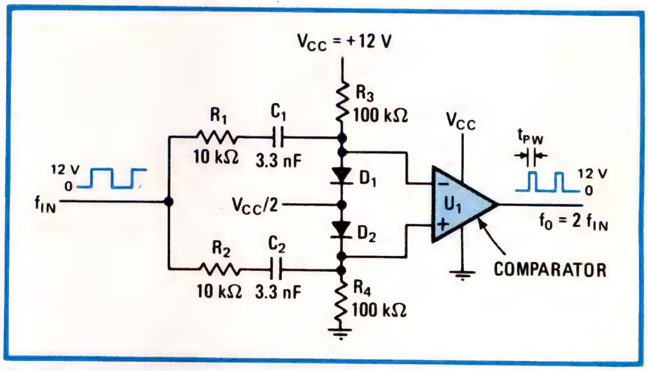
Single comparator forms frequency doubler

by Ralph A. Giffone
New England Research Laboratory, Cambridge, Mass.

Using just a single comparator chip and a few discrete components, this frequency multiplier produces rectangular pulses at twice the frequency of the input signal. The duration of the output pulses is adjustable and can be made asymmetrical by varying the rising and falling edges of the input signal. Also, the circuit is simple and may be built from off-the-shelf components.

The circuit (see figure) generates a positive pulse of duration t_{pw} on both the rising and falling edges of the input signal. On the rising edge, the inverting input terminal of the comparator is set at $0.5V_{cc}+0.6$ volt by D_1 while the noninverting input terminal rises to the full input voltage. Consequently, the comparator output goes high and remains in that state until C_2 charges to the level where the noninverting terminal is again less than $0.5V_{cc}+0.6$ V. On the pulse's falling edge, the positive terminal of U_1 is set to $0.5V_{cc}-0.6$ V by D_2 and the negative terminal is grounded. Again U_1's output goes high and remains so until C_1 charges to a point where the negative terminal is greater than $0.5V_{cc}-0.6$ V.

Since the input is a square wave and both sections of the circuit are identical, the durations of the output pulse for both the rising and falling edges of the input are the same. In terms of the component values, pulse width $t_{pw} = K(R_1+R_3)C_1$, where K is a constant that is dependent on V_{cc} and the input voltage. ☐



Doubler. Single comparator U_1 and a few discrete components yield a frequency doubler that generates a positive pulse of duration t_{pw} on both the rising and falling edges of the input signal. The duration of the pulse (t_{pw}) is adjustable and is given by $K(R_1+R_3)C_1$ for the falling edge and $K(R_3+R_4)C_2$ for the rising edge. For the components shown, t_{pw} measures about 0.31 ms.

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Highly integrated 16-bit microprocessor ups performance, aids design of work station

A personal professional work station, a typical application, is easy to build with the processor and a few other chips

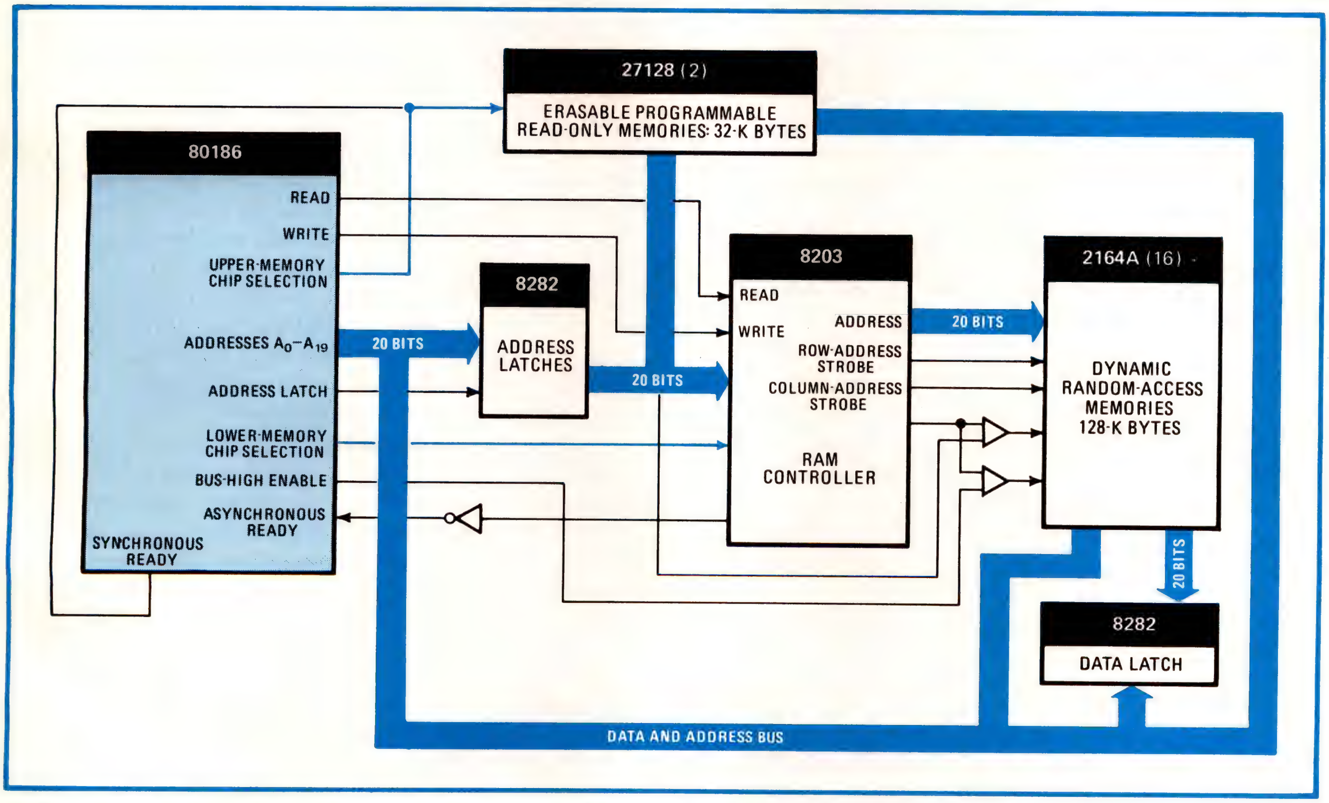
PART 2

This is the second article in a two-part series, and it discusses system design with the highly integrated 80186 microprocessor, focusing on the example of a personal work station for business use. The first article, appearing in the last issue, dwelt on the details of the 186's features and architecture. Although the 80186, also called the iAPX 186, was announced last year, this series is the first in-depth discussion of the architecture and how to design with it.

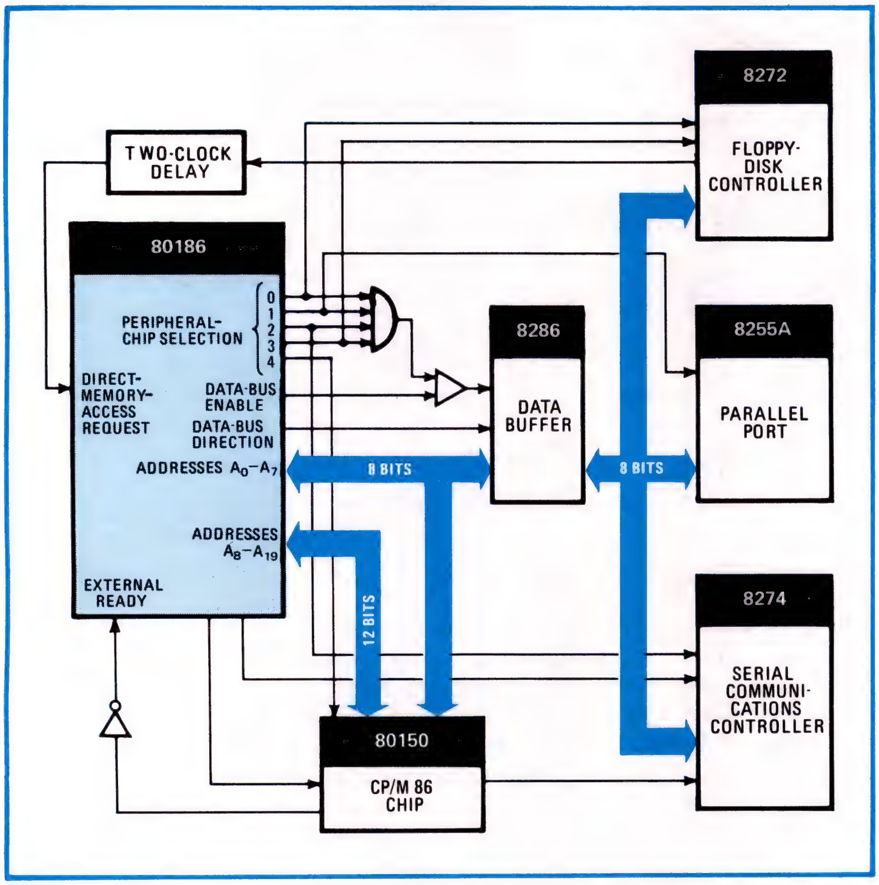
by Kenneth Shoemaker, *Intel Corp., Santa Clara, Calif.*

☐ Microprocessor makers are bringing a new guest to the party, and system designers are celebrating. The manufacturers have been using the advent of very large-scale integration to produce processor chips with many more integrated peripheral functions than ever before, thus making it possible for designers of work stations and personal computers to obtain the highest possible performance with the greatest number of features at the lowest possible cost.

One such processor is the iAPX 186, also known by its part number, 80186. Besides its 8086-compatible central processing unit, it contains a direct-memory-access controller, an interrupt controller, timers, chip-selection and wait-state circuitry, and a clock generator, so that it suits applications where component count, board size, and cost are primary design considerations. The low cost of VLSI designs like the 186 makes it possible to expand upon the set of features commonly expected in work stations and personal computers. Today these systems typically include a 16-bit microprocessor, at least 64-K



1. Memories. A typical memory subsystem for a personal work station's computer that is based on the 80186 microprocessor contains 16 dynamic random-access memory chips with their controller and two 27128 128-K erasable programmable read-only memories. Also part of the memory subsystem, but not shown here, is the memory portion of the 80150 CP/M 86 operating-system kernel, which is 16-K bytes of ROM.



2. Peripherals. An 80186-based system might have a set of peripheral chips including a floppy-disk controller, a parallel port, and a serial-communications controller. An 80150 chip, if included, would provide fast access to the CP/M 86 operating-system kernel.

bytes of random-access memory, a couple of floppy-disk drives, one or two serial-communication ports, and usually a parallel input/output port driving a printer.

Compatibility with existing application software and the bulk of new software being produced is almost always a high priority in such computer systems. The 186 fills these requirements because it is completely software-compatible with the 8086 and 8088 microprocessors, which have been used in many recent personal computers and work stations.

Designing a work station

Typical of the systems that can take most advantage of the performance and cost benefits of the 186 is a personal work station for business use. Such a design demonstrates how much the design process is simplified with the highly integrated 186. The integrated circuits used to provide the complete capabilities of this work station include an 8-megahertz 80186, an 8274 dual-channel synchronous and asynchronous serial controller, an 8272 floppy-disk controller, the 80150 CP/M 86 operating-system kernel, an 8255A 24-line parallel-I/O port, an 8203 84-K dynamic RAM controller with sixteen 2164A-20 (200-nanosecond) RAMs, and two 27128 128-K erasable programmable read-only memories.

The 186 microprocessor bus is almost identical to the 8086 bus. It features a multiplexed address and data bus and various control and status lines. These include read and write lines, a valid-address latch signal, a data-bus–direction signal, and a data-bus–enable line. It also has three status lines used to differentiate the bus cycles. The control and status lines may be connected to either a 8288 bus controller or a 8289 multimaster bus arbiter, which will be used in large 186 systems. The type of bus-exchange protocol in the 186 allows easy interfacing with the new generation of Intel peripheral devices, such as the 82586 Ethernet controller and the 82730 alphanumeric text coprocessor.

The 8-MHz 186 requires medium-speed memory and high-speed peripheral devices if it is to operate without wait states. However, it can be programmed to insert wait states automatically for simple interfacing with slower memory or peripheral devices. This provision simplifies system design when slow devices are used, since no external circuitry is required for adding wait states.

Because the 186 is really an enhanced version of the 8086, the functions of certain memory areas are predefined. The processor begins execution at location $FFFF0_{16}$, so this location will usually hold a nonvolatile-memory address such as an E-PROM containing the initialization code. Since the 186 uses the memory space defined by addresses 0_{16}–$3FF_{16}$ for an interrupt-vector table, this area is usually filled with RAM addresses. All other locations in the system memory can be used for operating-system code and users' application programs.

The integrated chip-selector and wait-state generator on the 186 supplies six signals for selection among the memory components in the system and for automatic insertion under program control of up to three processor wait states when an access is made to a particular memory device. The result is a considerable simplification of the circuitry for memory-chip selection.

In a typical memory system (Fig. 1), the chip-selection lines of the 186 select various memory banks. For example, the two E-PROMs, which include the power-on initialization code beginning at address $FFFF0_{16}$, are selected with the upper-memory chip-selection line. The lower-memory chip-selection line selects the entire bank of dynamic RAMs.

Though the E-PROMs and the 80150 memory do not require any wait states for proper operation, the RAM bank requires three of them for standard operation and additional time if a processor-to-memory access collides with a RAM refresh.

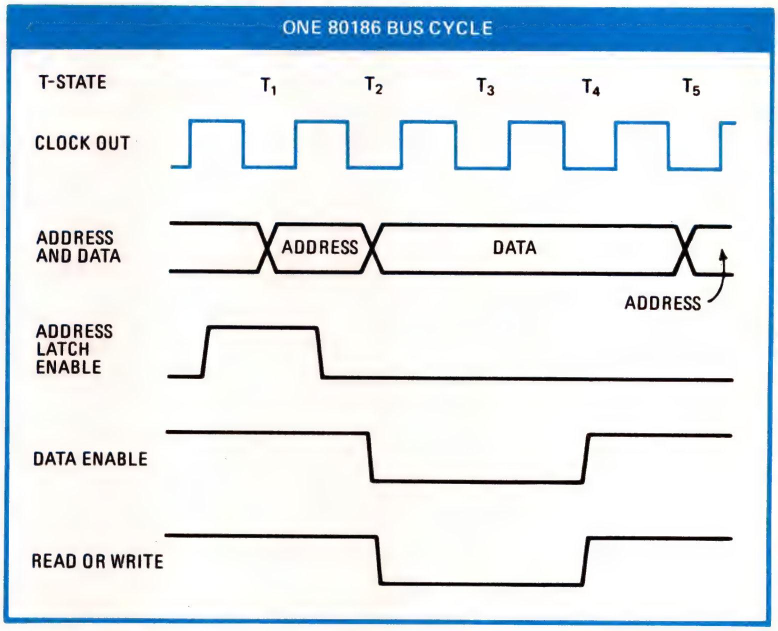
The reason for the three wait states, which slow down the interface, is the nature of the asynchronous 8203 RAM controller chosen for this design example. Much time is lost during every bus cycle to the memory bank

Interfacing with the 80186 bus

The 80186 single-chip microprocessor has a high-performance bus cycle with four clock periods, called time or T states. In performing a data transfer, different actions occur in each T state (see figure). Some devices may require additional time beyond the four-period cycle to drive the processor or to receive information from it. The additional time is obtained by inserting wait T states between cycles T_3 and T_4.

These wait T states may be inserted automatically by the integrated wait-state generator or by external logic driving the synchronous or asynchronous ready lines of the processor. The table shows the read access times for devices with various numbers of wait states connected to the 186 bus.

Another possible complication is bus contention after a read from a slow peripheral device. After the microprocessor performs a read operation from a device, it will drive the read-control line high. This step signals the external device to disable its data-output drivers. The 186 will then begin to drive address information onto the bus for the next T state no sooner than 85 nanoseconds after the read line has been driven inactive. If the external device cannot disable its output drivers within 85 ns, there could be bus contention between the 186 when it is driving address information for the next cycle and the external device when it is driving data information from the previous cycle. This problem is solved by placing a data buffer between the peripheral device's data lines and the microprocessor's bus.



resolving the asynchronous signals from the processor to the RAM controller. Alternatively, a synchronous RAM controller such as the 8207 would yield higher performance if needed. The response time of the memory bank to accesses from the 186 would be much faster because fewer or no wait states would be required.

Since the 186 multiplexes both addresses and data over its external bus, addresses must be latched into external devices if they are to remain stable during a bus cycle. Few memory devices have such latches. A typical 186 system will require separate transparent address latches, which minimize the time between the arrival of a valid address from the processor and its presentation to memory. The address-latch signal from the 186 allows simple latching of valid addresses into external registers.

Although data and address information share the processor bus, performance is not penalized, since data and addresses are moved on the bus during completely independent time cycles. Also, the requirement for external address latches does not complicate system design because address information must go to a variety of memory and I/O devices that are likely to require some buffering anyway.

The 186's memory is arranged as 16-bit words; however, it can also be accessed as individual 8-bit bytes. This duality means that a memory write operation can modify either the entire word or just the upper or lower byte. To access each byte of a word separately, the system needs a mechanism to enable only the correct half of memory during a byte write. The 186 provides two signals to control writing to either half of memory or to both at once. Such a technique is unnecessary during byte reads, for both halves of the memory may be accessed and the unused byte discarded.

External ready lines are either automatically assumed to be ready or are ignored by the processor or are used to insert additional wait states after the integrated wait-state generator has inserted the programmed number of wait states. Because the wait-state generator can be programmed to ignore external ready lines, they need not be driven ready by devices that require a fixed number of wait states, such as E-PROMs, most static RAMs, and most I/O peripheral devices. The correct number of programmed wait states is always generated for these parts, thus simplifying the ready circuitry of 186-based systems.

Peripheral grouping

The 8274 serial-communications controller, 8255A parallel port, and 8272 floppy-disk controller in this design for a work station may be considered as a group because they are all addressed the same way. Since the external data bus is 16 bits wide, these 8-bit peripheral devices reside only on the bus's lower half, the even half. The sequential registers of the peripheral chips will reside at subsequent even addresses, 400_{16}, 402_{16}, and so on.

A sample peripheral system (Fig. 2) requires a data buffer like an 8286 or 8287 to prevent bus contention between the 186 processor and the peripheral devices (see "Interfacing with the 80186 bus," p. 145). The processor provides two lines to control the enabling of the buffer and the data direction. The data-bus–direction line is directly connected to the transmit line of the buffer, while the data-bus–enable line is joined with the peripheral-selection lines of the processor such that it is enabled only when an access is made to a peripheral device.

This interdependency is required because the data-bus–enable line is driven active during all bus cycles when data is active on the bus. If the peripheral-chip–selection lines were not factored into the buffer-enable control line, the buffer would drive the 186 bus during any read cycle, whether to the peripheral devices or to memory. This intervention would cause bus contention between the peripheral buffer and the memory system.

The 186's peripheral-chip–selection lines directly select the individual peripheral devices. These seven lines activate seven contiguous 128-byte locations above a programmable base address. This base address may be either in I/O space or in memory space, so that the peripherals may be mapped as I/O or memory under program control. In addition, whenever any of the peripherals is selected by the 186, the integrated wait-state generator will insert the required number of wait states to ensure that good data is written to or read from the device.

The floppy-disk controller uses the DMA unit on the 186 to provide high-speed I/O from and to the disk. The controller requests a transfer for every byte of data, and the DMA controller accesses consecutive bytes in memory from either the upper or lower half of the data bus, thus handling both the sequential access of 8-bit data from the disk and putting 16-bit data in the memory.

The 186 DMA controller does not return an acknowledgment signal. The DMA acknowledgment is just the writing or reading of data to or from the requesting device. The acknowledgment can be handled this way because every DMA cycle on the 186 will require two bus cycles—one to fetch the data, the second to deposit it.

An explicit DMA acknowledgment is required only when data is passed from an I/O device to the memory in a single bus cycle. Because the disk controller requires both chip-selection and DMA-acknowledgment signals, two of the 186's peripheral-chip–selection lines are dedicated to providing them. Whenever the processor wishes to read or write control information to the floppy-disk controller, it accesses the address corresponding to its chip-selection line connected to the controller's chip-selection line. Whenever the DMA unit needs to read or write data in response to a request, it accesses the processor's chip-selection line that is connected to the controller's DMA-acknowledgment line.

The integrated DMA controller can gain control of the processor bus much more quickly than an external controller could. The result is better system performance, because fewer clock cycles are wasted during the bus transfer between the CPU and the DMA channel. However, this speed can cause problems with some peripheral devices that require a minimum time between the request for a direct-memory access and the DMA unit's acknowledgment. For example, the 8272 floppy controller requires 800 ns between request and acknowledgment, while the DMA controller can respond in as little as 625 ns. The problem is solved by inserting two clock cycles of delay between the disk controller's DMA request-line output and the DMA controller's request-line output.

READ ACCESS-TIME REQUIREMENTS FOR 80186

Number of wait states	Read access time (ns)
0	311
1	436
2	747
3	1,058

Operating-system chip

This example of a personal work station based on the 186 uses the 80150 for its CP/M 86 operating-system kernel. This chip supplies the system with an additional interrupt controller and additional timers. Because the 186 bus is almost identical to the 8086 bus, the 80150 attaches to the 186 without any glue chips.

The 8274 serial-communications controller uses the timer unit on the 186 to provide the baud-rate clock for one of its serial channels. It uses the baud-rate timer on the 80150 to provide the clock for the other channel. Both clock sources can be programmed to deliver a continuous stream of pulses with the proper spacing for the required baud rate. However, different programming sequences are needed to initialize the two clock sources.

The acknowledgment line from the 80150 is connected to the external ready line of the microprocessor so that whenever any resource on the former is accessed, an external ready signal is returned to the latter. This return signal is not, however, required for accesses to the 80150's 16-K ROM or its integrated peripheral devices. The chip-selector and wait-state generator on the 186 can be programmed to ignore all external ready signals when accessing such a chip and to terminate the bus cycle regardless of the state of the external ready.

The system initialization code must set up the control registers of the microprocessor's chip-selector and wait-state generator. The only chip-selection line that will be active before being explicitly initialized by the CPU is the upper-memory selection line, and it will be active only during access to the top 1-K of memory space. When the the integrated chip-selection unit is used and the program jumps the top 1-K of the address space before the related registers are properly programmed, the system will not operate because the memory-selection line will not be driven active.

All that the initialization code (see table) need do is determine the number of wait states required for the various devices in the system and then insert the appropriate programmed values. After the chip-selection lines are initialized, the rest of the system may be initialized in any order the system designer wishes. ☐

Shallower streaming-tape drives promise compact mass-storage backup

Also newly capable of storing 600 megabytes, the 1/4-inch-tape cartridge is becoming a more competent helpmate for Winchester disks

by M. Thomas Makmann, *Archive Corp., Costa Mesa, Calif.*

☐ Both now and for the foreseeable future, Winchester disk drives will be the primary mass-storage device of the personal and professional computer. But their backup devices have failed to keep up with the unique ability of these drives to combine ever smaller physical sizes with ever greater bit capacities—10 or more megabytes apiece in the newest personal computer systems.

Quarter-inch streaming-tape drives are now making a strong bid for that backup role. Today they are capable of storing 60 megabytes on a single cartridge containing 600 feet of tape. With a tape speed of 90 inches per second, such a peripheral is ideal for supporting Winchester disks in the 10-to-over-200-megabyte range. In addition, these drives can perform the typical tasks required by a removable-medium device, like software distribution, program interchange, and program and system loading.

Left behind

In contrast, floppy-disk drives have, at any rate for the time being, dropped out of the contest. At least until the further development of vertical recording, they seem unlikely to advance beyond a 1-megabyte limit in capacity—indeed an inadequate backstop for hard-disk storage that can reach 300 megabytes. Moreover, their small size, perhaps their strongest claim to use in desktop computer applications, has now been duplicated by the latest and smallest streaming-tape device, the Scorpion from Archive Corp. (Fig. 1). It has the form factor of a half-height, 5¼-in. floppy-disk drive, yet it is capable of attaining a capacity of as much as 60 megabytes.

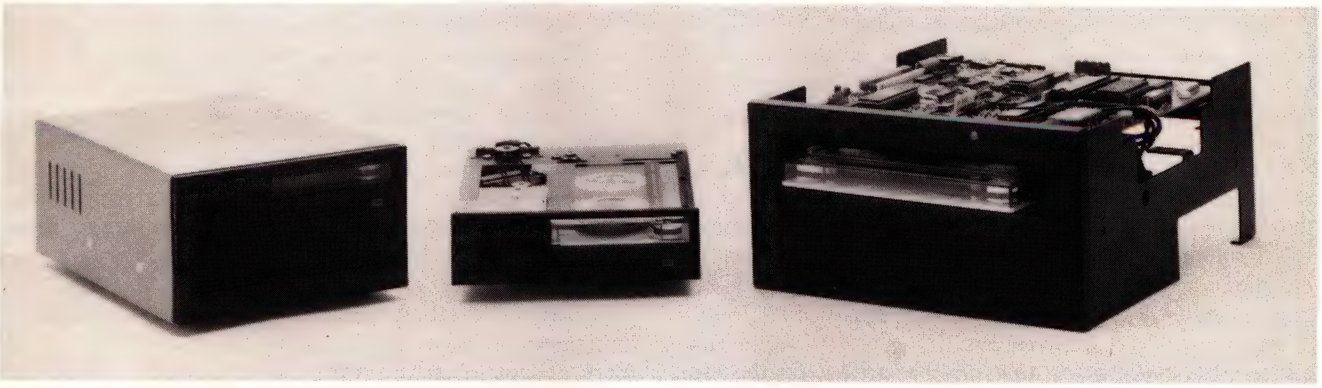
An alternative backup for Winchester disks is the ½-in. tape drive, which is popular for archival and backup systems in minicomputer and larger installations. But it has not progressed beyond the 6,250-bit-per-inch group-coded recording introduced a decade ago. In the next couple of years, the system designer and end user can expect to see continuing dramatic increases in capacity—or decreases in size—for the Winchester disk as well for the 1/4-in. streaming-tape drives. Stated another way, the smaller systems and peripherals will become as powerful as their larger counterparts.

Contents first

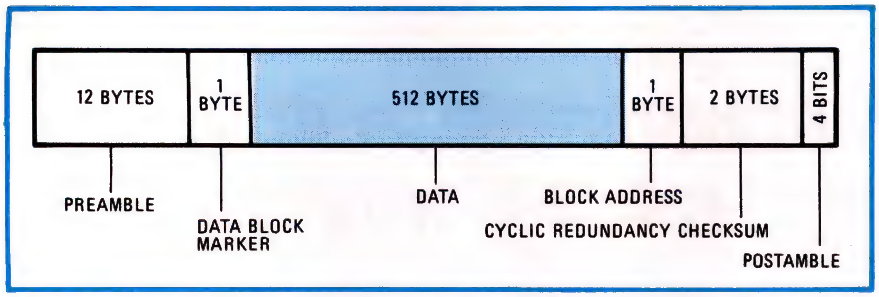
But any description of just how the Scorpion streaming-tape cartridge was shoehorned into a small floppy-disk–style package deserves to be justified in terms of the ultimate utility of the approach. A closer look at the Scorpion and its very similar predecessor, the Archive Sidewinder, will show how well they serve the backup mass-storage needs of present and upcoming professional computer systems.

The Sidewinder is a 20-, 45-, or 60-megabyte tape drive packaged in an industry-standard 8-in. floppy-disk form factor. Its integrated intelligent formatter and controller relieve the host system of the jobs of tape motion control, tape formatting, and error-processing routines normally performed by separate device controllers or host software.

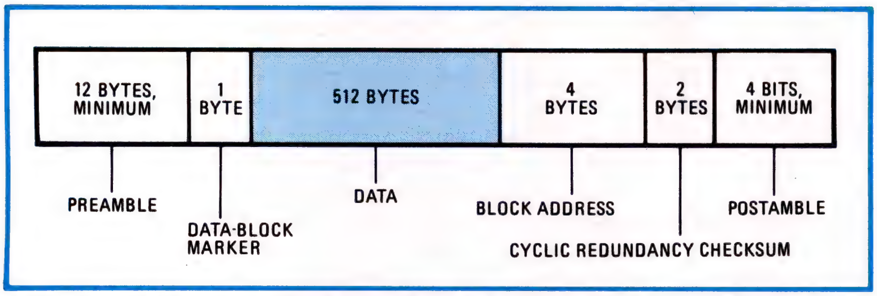
The tape format for the current 8-in. Sidewinder prod-



1. The right size. The Scorpion 5.25-in. streaming-tape drive (middle) fits into exactly the same space as half-height 5.25-in. Winchester or floppy-disk drives. It is a much better match for small systems than 8-in. drives (right). A full-height 5.25-in. streamer with controller is shown at left.



2. Efficient. The Archive tape format employed in the 8-in. Sidewinder tape drives uses the tape efficiently. Within each 528.5-byte block, 512 bytes are used for data, yielding 97% efficiency. The 5.25-in. Scorpion product can use either this format or the QIC-24 format.



3. New format. A new format, QIC-24, has been defined for the 5.25-in. drives. It is a modified version of the Archive format shown in Fig. 2. A track-reference burst was added before track zero and the block-address field was increased from 1 byte to 4 for extended addressing.

uct (Fig. 2) is a fixed 512-byte data field with a single-byte block address and a 2-byte cyclic redundancy checksum. Together with the 12.5-byte interblock resynchronization burst, composed of the preamble and the postamble, and the 1-byte data-block marker used as a synchronization character, this becomes a 528.5-byte block. A block of this length containing a 512-byte data field yields a 97% tape utilization factor. File marks are also written as full 528.5-byte blocks with a unique character used as a file marker written in the data field.

The present 8-in. product has been in production for a number of years and, with tens of thousand of units in the field, has become a considerable force in the industry. Its companion product, introduced just recently, is the Scorpion with (as already noted) a form factor matching that of a half-height 5.25-in. floppy-disk drive.

The Scorpion uses the same industry-standard 450-foot–tape cartridge as the Sidewinder and has comparable 20- and 45-megabyte capacities. In addition, this product can use the recently announced DC600 cartridge, which contains 600 ft of tape. This 30% longer tape boosts the nine-track version to 60 megabytes. The drive automatically detects and adjusts to the length of tape in the cartridge inserted.

In addition to the Archive standard tape format, the Scorpion drive is capable of reading and writing the newly defined QIC-24 tape format (Fig. 3). This format is a modified version of the original Archive format. The changes are a track-reference burst prior to track zero and an increase of the block address field from 1 byte to 4 because a 1-byte address does not yield a unique block address for every block that can be written on the tape. This 4-byte field is divided among three functions: 2.5 bytes for the block address, 1 byte for the track address, and 0.5 byte for optional features. The Scorpion drive can be commanded by software to write either format and will automatically determine which format is recorded on an existing tape.

But by far the dominant characteristic of the Scorpion drive is its physical size—half the height of a standard 5.25-in. disk drive. The entire set of functions of the 8-in. Sidewinder product is contained in that much smaller form factor. Mounting holes and front-panel bezel dimensions are also the same as for standard half-height 5.25-in. floppy-disk drives.

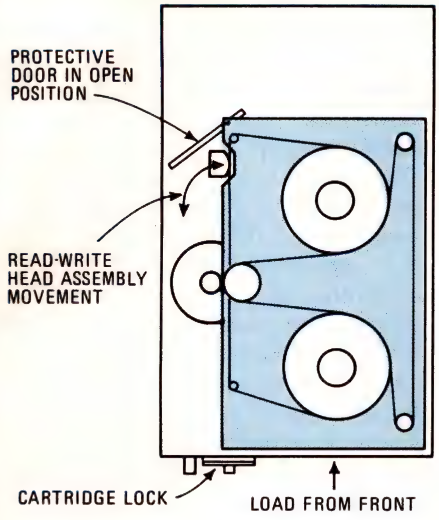
The 5.25-in. tape drives, like their 8-in. counterparts, are ideal for doing Winchester disk backup, program loading and distribution, and other removable-media functions. They also fit extremely well into the shrinking systems of today and offer the system designer increased capability and value for the systems of tomorrow.

The reduction in the Scorpion's physical size is made possible by two major design efforts—large-scale integration and mechanical packaging. The mechanical design behind fitting a 5.25-in. cartridge tape drive into the half-height floppy-disk–drive form factor presented a challenging task. To start with, the industry-standard American National Standards Institute cartridge used in these products was not meant for a 5.25-in. enclosure. It was designed for loading the tape front first, such that the read-write head and capstan are easily engaged.

But, to fit within the 5.25-in. form factor measurements, the cartridge must be loaded short side first rather than front first (Fig. 4). Now, though, it is no longer easy to engage the read-write head and capstan because, with its protective door open, the cartridge width is equal to the inside width of the 5.25-in. enclosure. Consequently, there is no room left for the read-write head to simply slide forward.

Instead, a more complex loading method was designed to open the protective door, move the read-write head into position, and engage the capstan. Also, to ensure reliable operation and media interchangeability, the load mechanism must reference the cartridge to the ANSI-defined cartridge-reference surface, and the mechanical tolerances in positioning the read-write head must be accurately controlled.

A number of packaging methods with varying degrees of acceptability were considered during the design phase. The entire mechanism could have been pulled out from its enclosure and the tape loaded front first from the side. But this method has serious packaging and esthetic limitations and would be unlikely to be acceptable to all users. All other methods evaluated loaded the tape cartridge endwise through the front of the unit and moved the mechanical assemblies out of the way for loading and


PROTECTIVE DOOR IN OPEN POSITION
READ-WRITE HEAD ASSEMBLY MOVEMENT
CARTRIDGE LOCK
LOAD FROM FRONT

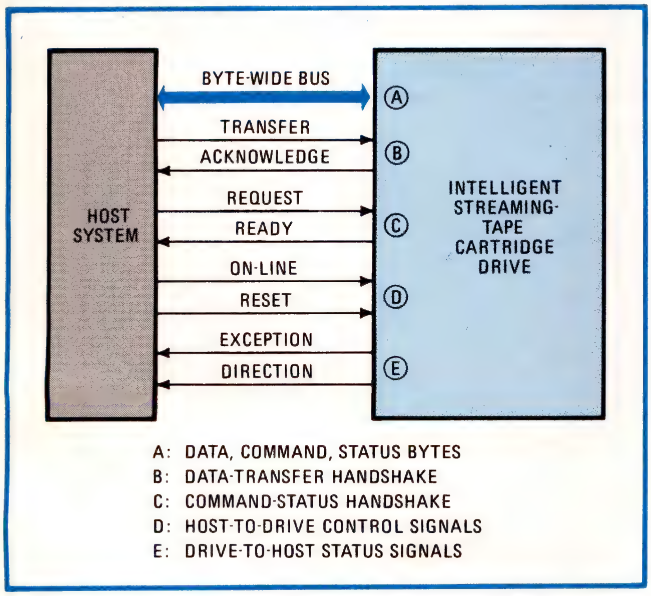
CARTRIDGE LOADING AND UNLOADING SEQUENCES

Operation	Action
TO LOAD:	
Insert tape cartridge.	Opens protective door, loads eject spring, and references cartridge.
Move front panel slide lever to right.	References cartridge, loads head assembly, and locks cartridge in place.
TO UNLOAD:	
Move front-panel slide lever to center.	Unloads head assembly.
Move front-panel slide lever past center.	Closes protective door Ejects cartridge part way.

4. Side slip. The physical dimensions imposed on the tape cartridge by the 5.25-in. floppy-disk–drive form factor required a mechanical design where the tape is loaded side or end first, rather than front first, as is conventional. This meant that the protective door on the cartridge would have to be opened and the read-write head assembly brought into position after the cartridge had been fully loaded.

then back into position to engage the read-write head assembly and tape capstan. In the final packaging developed by Archive, once the tape cartridge is loaded it does not stick out anywhere at anytime. The cartridge loading and unloading sequence is shown in Fig. 4.

The printed-circuit board area available in the 5.25-in. product is significantly less than in the 8-in. product. The basic Scorpion drive and the version with the built-in formatter and controller both make extensive use of state-of-the-art LSI to provide the same functions in a smaller package. Most of the formatter and controller logic has been incorporated into proprietary integrated circuits. As well, numerous hybrid circuits are used to further reduce the chip count. Other advantages of an LSI implementation are smaller size, lower power consumption, and increased reliability.


HOST SYSTEM
BYTE-WIDE BUS
TRANSFER
ACKNOWLEDGE
REQUEST
READY
ON-LINE
RESET
EXCEPTION
DIRECTION
Ⓐ
Ⓑ
Ⓒ
Ⓓ
Ⓔ
INTELLIGENT STREAMING-TAPE CARTRIDGE DRIVE
A: DATA, COMMAND, STATUS BYTES
B: DATA-TRANSFER HANDSHAKE
C: COMMAND-STATUS HANDSHAKE
D: HOST-TO-DRIVE CONTROL SIGNALS
E: DRIVE-TO-HOST STATUS SIGNALS

5. Interface. The proposed standard interface for 1/4-in. streaming-tape cartridge drives called QIC-02 Rev D uses an asynchronous protocol over a byte-wide bidirectional bus. Other lines are used for handshakes, control, and other status signals.

There is one area, however, where the system designer or end user would prefer to see no change. This is at the interface of the new peripheral with the system. Once a peripheral type has been integrated into a system and the hardware and software interfaces are fixed, subsequent products should adhere to the same interfaces.

Standard interfaces

Considerable progress has been made on standardizing an interface for the 1/4-in. streaming-tape drive. The QIC group (Quarter-Inch Cartridge Drive Compatibility Committee) has produced an interface specification referred to as QIC-02 Rev D that defines a device-level interface for connecting the drive to its controller [*Electronics*, May 5, 1983, p. 110]. The specification document defines the interface parameters and command set that must be implemented to be plug-compatible with the QIC-02 interface. A number of optional commands have been defined as well and can be implemented as required.

The QIC-02 interface (Fig. 5) uses an asynchronous handshake protocol and a byte-wide bidirectional bus for command, status, and data transfers. All standard commands are initiated by the transfer of a byte-wide command from the host to the drive. The QIC committee has also defined a specification called QIC-24 for data interchange that defines the data format and track positions on the tape.

In the case of the intelligent Scorpion, its interface with the host is the same QIC-02 Rev D one as is used by the 8-in. Sidewinder drives. Therefore the new drives can be easily added to existing systems since existing host adaptors and host software need not be changed. In addition, a number of QIC-02 optional commands will be implemented in the peripheral device to enhance its capability. ☐

8031's counter buys it a bargain 16-bit a-d converter

by Akavia Kaniel
Intech Inc., Santa Clara, Calif.

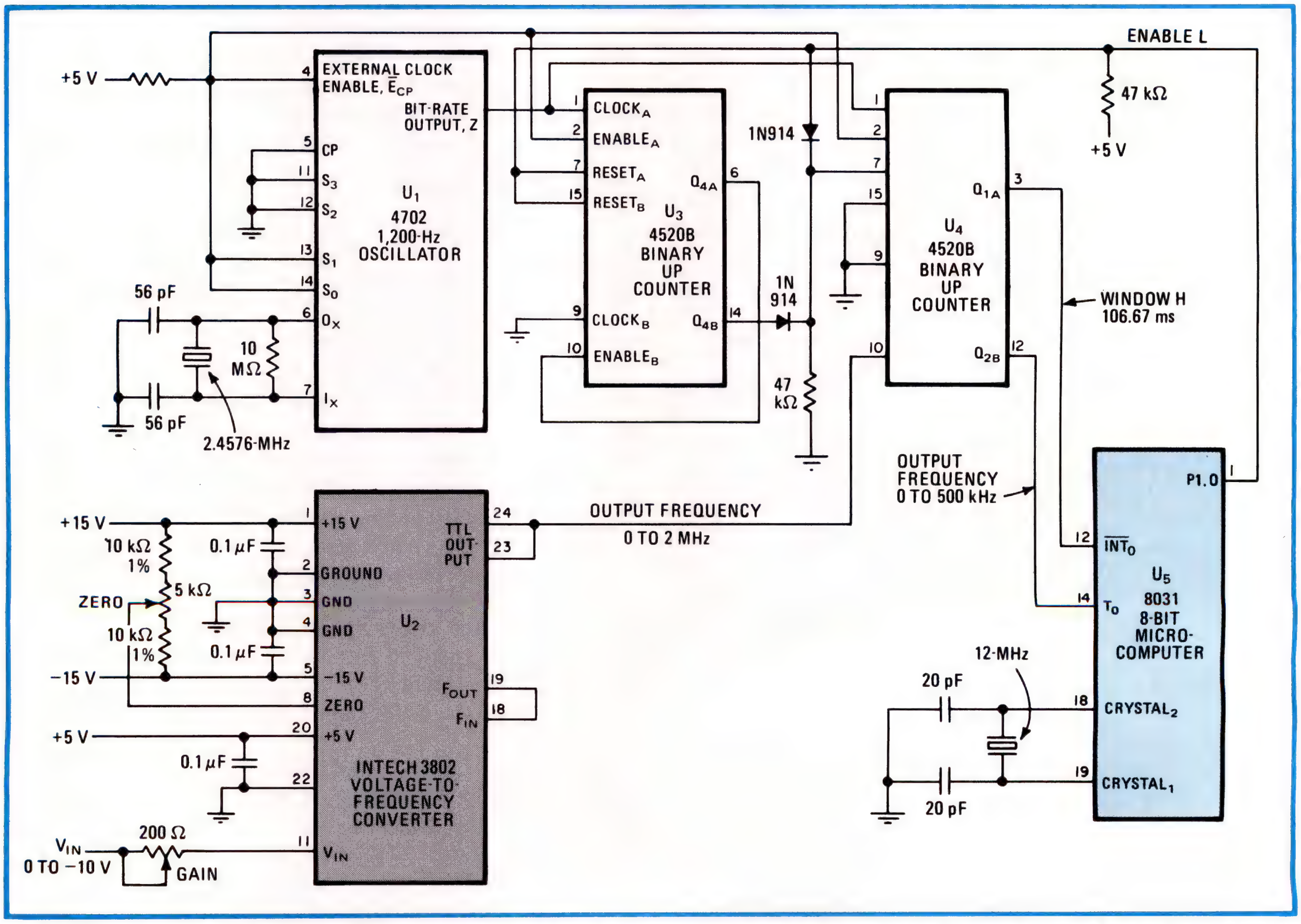
The Intel 8031 microprocessor's on-chip 16-bit counter, together with an Intech or Dynamic Measurements Corp. 3802 voltage-to-frequency converter, equips the appropriately programmed 8031 with an inexpensive high-resolution 16-bit analog-to-digital converter that is simple to construct. Other advantages of the design are an inherently monotonic transfer function, no missing codes, integration of noise during conversions, and no reference phase (so that the converter can start the next conversion immediately upon concluding the previous one).

Voltage-to-frequency converter U_2 tracks input voltage V_{in} (see figure), which is between 0 and –10 volts, and produces a continuous pulse stream having a frequency proportional to the input voltage. For the input voltage shown, the voltage-to-frequency converter's output frequency is between 0 and 2 megahertz. Binary counter U_4 divides this frequency by 4 to produce a 0-to-0.5-MHz output.

Whenever the microprocessor is ready to start a conversion, it pulls the enable-L line low and opens the fixed time window H for 106.67 milliseconds. During this time, the pulses at the output of the voltage-to-frequency converter are counted by the 8031's 16-bit counter, which is enabled by the window pulse. As a result, a digital number proportional to the input voltage is generated. Once the window closes, the counter is disabled and the microprocessor is interrupted.

The 8031's a-d conversion program indicates that when the processor is interrupted, it halts the window generator by pulling the enable-L line high. The microcomputer then reads the conversion result stored in the counter, clears the counter, and starts the next conversion. The 106.67-ms window pulse is generated by the crystal-controlled window generator that is composed of 1,200-hertz oscillator U_1, binary counters U_3 and U_4, and the 8031's 12-MHz clock. ☐

Software notebook is a regular feature in *Electronics*. We invite readers to submit short, original, unpublished programs and software solutions to engineering problems. Explain briefly and thoroughly the program's operation. We'll pay $75 for each item published.



A-d converter. Using the a-d–conversion program for Intel's 8031 and a voltage-to-frequency converter U_2, this design offers the 8031 a simple 16-bit a-d converter. U_2 converts the analog input into a pulse train counted by the 8031's 16-bit counter within a time window.

8031 PROGRAM FOR ANALOG-TO-DIGITAL CONVERSION

```
; ASSIGN SECTION – ASSIGNS LABELS TO HARDWARE ADDRESSES.
;
            ENABLE    BIT       P1.0          ; ASSIGNS THE NAME ENABLE
                                              ; TO INPUT/OUTPUT PIN P1.0 OF THE
                                              ; MICROPROCESSOR.
            DSEG
            CTR_LSB DATA        20H           ; STORAGE LOCATION FOR LEAST SIGNIFICANT BYTE
       ; BYTE OF THE COUNTER.
CTR_MSB DATA 21H   ; STORAGE LOCATION FOR MOST SIGNIFICANT BYTE
       ; BYTE OF THE COUNTER.
;
; INTERRUPT SERVICE ROUTINE –
;
; THE MICROPROCESSOR WHEN INTERRUPTED BY THE TRAILING EDGE OF THE WINDOW-H
; PULSE, VECTORS TO LINE 3 OF THE PROGRAM MEMORY.
;
            CSEG
            ORG       03H
WND_IN:     JMP       DONE                    ; JUMP TO THE MAIN PROGRAM
                                              ; TO READ THE CONVERSION
                                              ; RESULT, IN THE COUNTER.
;
; INITIALIZE ROUTINE – PRESET THE MICROPROCESSOR.
;
INIT:       ORG       2AH
            SETB      ENABLE                  ; DISABLE THE WINDOW GENERATOR
                                              ; BY PULLING THE ENABLE-L LINE
                                              ; HIGH.
            MOV       TCON, =1H               ; ENABLE INTERRUPT ON EDGE.
            MOV       IE, =81H                ; ENABLE INTERRUPT 0
            MOV       SP, =30H                ; PRESET THE STACK POINTER.
            MOV       TL0, =0H                ; CLEAR THE LEAST SIGNIFICANT BYTE AND MOST SIGNIFICANT BYTE REGISTERS
            MOV       TH0, =0H                ; OF THE COUNTER.
            MOV       TMOD, =0DH              ; SET COUNTER 0 TO BE A 16-BIT
                                              ; COUNTER.
;
; MAIN ANALOG-TO-DIGITAL CONVERSION ROUTINE –
;
; ENABLES THE COUNTER IN THE MICROPROCESSOR. COUNT UNTIL THE END OF THE WINDOW-H
; PULSE AND READS THE COUNTER (ANALOG-TO-DIGITAL CONVERSION) RESULT.
;
START:      MOV       TCON, #11H              ; ENABLE THE COUNTER INTERNALLY
                                              ; IN THE MICROPROCESSOR.
            CLR       ENABLE                  ; ENABLE THE WINDOW GENERATOR BY
                                              ; PULLING ENABLE-L LOW.
WAIT:       JMP       WAIT                    ; WAIT HERE FOR THE INTERRUPT AT THE
                                              ; END OF THE WINDOW-H PULSE.
DONE:       SETB      ENABLE                  ; DISABLE THE WINDOW GENERATOR BY
                                              ; PULLING ENABLE-L HIGH.
            MOV       TCON, #0H               ; HALT THE COUNTER INTERNALLY.
            MOV       CTR_LSB, TL0            ; READ AND CLEAR THE LEAST SIGNIFICANT BYTE OF
            MOV       TL0, #0H                ; THE COUNTER.
            MOV       CTR_MSB, TH0            ; READ AND CLEAR THE MOST SIGNIFICANT BYTE OF
            MOV       TH0, #0H                ; THE COUNTER.
```

8048 program computes 16-by-8-bit quotient

by Donald W. McGuire
Red Lion Controls, York, Pa.

Many 16-by-8-bit divide routines for 8-bit microcontrollers yield an 8-bit result and an 8-bit remainder, thus forcing the divisor to be greater than the most significant byte of the dividend so that the result may be contained in 1 byte. But for many industrial applications, this restriction is intolerable.

The divide routine presented here for the 8048 microcontroller eliminates the above requirement by furnishing a 16-bit resultant and an 8-bit remainder. Yet it uses only the same number of registers as a typical 16-by-8-bit divide routine.

In the algorithm employed, the divisor is shifted left until the most significant bit is a 1 and the cycle counter, register R_5, is incremented once for each shift. Next the dividend is shifted left until the most significant bit of the high-order byte is a 1; the cycle counter is then decremented for each shift. The divisor is repeatedly subtracted from the higher-order byte of the dividend and the results shifted left. A 0 is added to the result if the subtraction generates a carry, a 1 if it does not do so. This process continues until the cycle counter is decremented to 0.

In order to facilitate simultaneous shifting of the dividend and the results, register R_2 and the accumulator are used to hold the result and the initial dividend. When R_5 reaches zero, the division process is complete and the remainder is separated from the quotient. The remainder, which is contained in the high-order byte of the results, is first brought to its proper significance by shifting it to the right until its least significant bit is located in bit 0 of the accumulator. ☐

8048 PROGRAM FOR 16-BY-8-BIT DIVISION

```
               ;
               ;
               ;         THIS IS A 16-BY-8-BIT DIVIDE ROUTINE THAT
               ;         PROVIDES A TWO-BYTE RESULT AND A ONE-
               ;         BYTE REMAINDER
               ;
               ;         AT ENTRY:
               ;         A  = UPPER 8 BITS OF DIVIDEND
               ;         R2 = LOWER 8 BITS OF DIVIDEND
               ;         R1 = POINTER TO DIVISOR IN RANDOM-ACCESS MEMORY
               ;
               ;         AT EXIT:
               ;         A  = UPPER 8 BITS OF RESULT
               ;         R2 = LOWER 8 BITS OF RESULT
               ;         R1 = POINTER TO REMAINDER IN RAM
               ;         C  = SET IF DIVISOR IS 0 OR
               ;              GREATER THAN THE DIVIDEND
               ;
               ;
               ;
               ;
0100  960A     DIVIDE    JNZ    DIVIDE1     ; THIS SECTION
0102  2A                 XCH    A, R2       ; TESTS THAT
0103  37                 CPL    A           ; THE DIVIDEND
0104  61                 ADD    A, @R1      ; IS GREATER
0105  37                 CPL    A           ; THAN THE
0106  61                 ADD    A, @R1      ; DIVISOR
0107  F653               JC     ERROR1
0109  2A                 XCH    A, R2
010A  21       DIVIDE1   XCH    A, @R1      ; TEST IF
010B  C652               JZ     ERROR       ; DIVISOR "0"
010D  BD01               MOV    R5, #01     ; PRELOAD COUNT
010F  F215     DIVIDE2   JB7    DIVIDE3     ; LEFTHAND JUSTIFY
0111  E7                 RL     A           ; THE DIVISOR
0112  1D                 INC    R5          ; INCREASE CYCLE
0113  240F               JMP    DIVIDE2     ; COUNT
```

```
00045  0115  19     DIVIDE3   INC   R1           ; STORE
00046  0116  2D               XCH   A, R5        ; COUNT
00047  0117  A1               MOV   @R1, A       ; IN RAM
00048  0118  0308             ADD   A, #08       ; INCREASE
00049  011A  2D               XCH   A, R5        ; COUNT BY 8
00050  011B  C9               DEC   R1
00051  011C  85               CLR   F0
00052  011D  21               XCH   A, @R1
00053  011E  F227   DIVIDE4   JB7   DIVIDE5      ; LEFTHAND
00054  0120  97               CLR   C            ; JUSTIFY THE
00055  0121  2A               XCH   A, R2        ; DIVIDEND
00056  0122  F7               RLC   A
00057  0123  2A               XCH   A, R2        ; DECREASE
00058  0124  F7               RLC   A            ; CYCLE
00059  0125  ED1E             DJNZ  R5, DIVIDE4  ; COUNT
00060  0127  37     DIVIDE5   CPL   A            ; SUBTRACT DIVISOR
00061  0128  61               ADD   A, @R1       ; FROM MOST SIGNIFICANT BYTE OF
00062  0129  37               CPL   A            ; DIVIDEND
00063  012A  E62F             JNC   DIVIDE6      ; IT
00064  012C  B631             JF0   DIVIDE7      ; FITS
00065  012E  61               ADD   A, @R1       ; DOES NOT FIT
00066  012F  A7     DIVIDE6   CPL   C            ; PREPARE FOR SHIFT
00067  0130  95               CPL   F0           ; INTO RESULT
00068  0131  2A     DIVIDE7   XCH   A, R2        ; SHIFT CARRY
00069  0132  F7               RLC   A            ; INTO RESULTS
00070  0133  2A               XCH   A, R2
00071  0134  F7               RLC   A
00072  0135  E638             JNC   DIVIDE8      ; 1 SHIFTED
00073  0137  85               CLR   F0           ; INTO CARRY
00074  0138  95     DIVIDE8   CPL   F0           ; SET FLAG
00075  0139  ED27             DJNZ  R5, DIVIDE5  ; REPEAT
00076  013B  A1               MOV   @R1, A       ; SAVE HIGH RESULT
00077  013C  19               INC   R1           ; GET
00078  013D  F1               MOV   A, @R1       ; INITIAL
00079  013E  C9               DEC   R1           ; COUNT
00080  013F  AD               MOV   R5, A
00081  0140  F1               MOV   A, @R1       ; GET HIGH RESULT
00082  0141  67     DIVIDE9   RRC   A
00083  0142  97               CLR   C            ; RESTORE
00084  0143  ED41             DJNZ  R5, DIVIDE9  ; REMAINDER
00085  0145  21               XCH   A, @R1       ; SAVE IT
00086  0146  19               INC   R1           ; GET
00087  0147  21               XCH   A, @R1       ; INITIAL
00088  0148  2D               XCH   A, R5        ; COUNT
00089  0149  97     DIVIDEA   CLR   C
00090  014A  A7               CPL   C            ; REMOVE
00091  014B  F7               RLC   A            ; REMAINDER
00092  014C  ED49             DJNZ  R5, DIVIDEA  ; FROM
00093  014E  51               ANL   A, @R1       ; HIGH RESULT
00094  014F  C9               DEC   R1
00095  0150  97               CLR   C
00096  0151  83               RET
00097  0152  21     ERROR     XCH   A, @R1       ; SWAP DIVISOR/DIVIDEND
00098  0153  97     ERROR1    CLR   C
00099  0154  A7               CPL   C            ; SET CARRY
00100  0155  83               RET
00101                         END
```

Engineer's newsletter

It's official: Ada joins the military

The military's Ada programming language, now approved by the American National Standards Institute, **has been assigned the military standard designation ANSI/MIL-STD 1815A,** according to the Ada Joint Program Office. The office says copies of the standard can be requested on Department of Defense Form 1425 from the Commanding Officer at the Navy Publications and Form Center, 5801 Tabor Ave., Philadelphia, Pa. 19120. Organizations offering courses, seminars, training programs, and textbooks on Ada can get free publicity in a new quarterly catalog to be called Crease—for Catalog of Resources for Education in Ada and Software Engineering. Those wishing to be included should request questionnaires by calling (315) 336-2359 and asking for AdaIC.

What's what and who's who in surface mounting

Surface mounting of integrated-circuit packages and passive components to printed-circuit boards has become one of today's hottest topics. In "Surface Mounting Directory 1983," D. Brown Associates Inc. has produced a valuable aid for the actual or potential user of this technique. **This directory contains some 100 different categories, with over 6,000 component, equipment, and service listings,** well-organized and cross-indexed. Each of five product sections—components, sockets, specialized test handling equipment, assembly equipment, and contract services—contains four to five separate indexes that include product type and description, part number, package style, and packaging. Also included is an introduction to surface-mounting technology and a company index. The publication sells for $400. For information, contact Don Brown, D. Brown Associates Inc., P. O. Box 43, Warrington, Pa. 18976.

How to talk about superconductors

To compile a working vocabulary for superconductors, the National Bureau of Standards evaluated input from dozens of institutions around the world and has come up with "Standard Definitions of Terms Relating to Superconductors." Published by the American Society for Testing and Materials, item B713-82, **the terms compiled are divided into four categories: fundamental states and flux phenomena; critical parameters; fabrication, stabilization, and transient losses; and Josephson phenomena.** The work, which is intended to be useful in setting specifications for practical commodity exchange, is obtainable for $4 by writing to the ASTM at 1916 Race St., Philadelphia, Pa. 19103. Another publication available, "Standard Test Method for dc Critical Current of Composite Superconductors" (B714-82), covers criteria and practical techniques for determining the dc critical current with an error of less than 5%.

Software free for the asking

The Folklife Terminal Club, a Commodore users group, is making its software library available to owners of VIC, CBM, and Pet computers for a nominal copying and mailing fee of $10 per disk. **The club's archives contain more than 5,000 programs in the public domain** covering education, business, games, and utilities. The first disk that should be ordered is the catalog disk, which contains an automatic disk-cataloging program, a listing of all the available programs, and instructions. For more information, the club can be reached at Box 2222, Mount Vernon, N. Y. 10551, or by calling Bob Krebs at (914) 664-1222. **–Steve Zollo**

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Program-design language based on ANSI-standard Ada comes with program analyzer that checks code and feeds document generator

by Stephen Evanczuk, Microsystems & Software Editor

Presaging the widespread use of the Department of Defense's Ada programming language, a new software package called Byron from Intermetrics Inc. should ease Ada software development from the design stage through to a finished, fully documented product. By describing programs with an augmented version of Ada as standardized by the American National Standards Institute, software developers can employ Byron's analyzer program to ensure that their code follows the rules of Ada. Subsequently, they may create software documentation through Byron's document generator, which draws documentation information from the source code itself.

In large software projects, program development must proceed along carefully structured and monitored paths. In order to formalize their development approach, large software houses often write representations of software systems using a program description language, commonly referred to simply as PDL.

In a movement toward a standard PDL, Intermetrics exploited the standardization afforded by using Ada itself as the basis for Byron PDL, which adds several keywords (see table) to ANSI-standard Ada. By adding to Ada's inherent ability to specify and, of course, implement software, developers can create a PDL framework that may be filled during development to yield a full Ada implementation of the original design.

As the PDL representation of a software design evolves into working programs, the Byron analyzer checks for the use of proper Ada syntax, enforces Ada's strong type checking, and compares separately compiled modules for type consistency. To fulfill the needs of document generation, the analyzer checks that Byron keywords are used correctly. Finally, it builds a program library containing a representation of the source program in intermediate code (called Diana) but augmented with documentation drawn from the source code.

Reporter. Byron circumvents the tedious task of writing product documentation by producing reports from this program library. Intermetrics' document generator combines input from the library with a report template—an outline detailing the format of the desired document—to produce software documentation representing the most current state of the Ada programs.

For example, defense contracts specify delivery of software specification documentation in a standard form called a C5, detailed in MIL-STD-490. Intermetrics itself uses Byron with a special C5 template to produce C5 documents as part of its development of the Ada Integrated Environment for the U. S. Air Force. The template is included as one of the elements of the Byron package.

At the end of May, Byron will be available for IBM 370 computers. A standard version priced at $75,000 is capable of handling programs of a size limited only by the available memory and disk-storage resources. The company also offers Byron in a more limited version priced at $25,000 that processes up to 5,000 lines of Byron code. The company offers a 40% discount for additional licenses purchased at the same time.

Licensing includes installation on the purchaser's computer, a full set of documentation, and a year of maintenance including updates. Additional maintenance contracts are available following the first year.

According to John Pates, marketing manager at Intermetrics, the company is planning a version for DEC VAX computers. Although Intermetrics expects to have the VAX version in six months, Pates notes that the company is prepared to work on a contract basis if a purchaser should need it earlier.

Intermetrics Inc., 733 Concord Avenue, Cambridge, Mass. 02138. Phone (617) 661-1840 [338]

KEYWORDS USED IN BYRON PROGRAM DEVELOPMENT PACKAGE

Keyword	Description of associated documentation
ALGORITHM	Procedure used to solve problem
EFFECTS	Function performed by subprogram
ERRORS	Error messages and circumstances
INVARIANT	Properties that do not change over time
MODIFIES	Global variables possibly affected
NOTES	Host dependencies or limitations
OVERVIEW	Relation of subprogram to environment
RAISES	List of exceptions that may be raised
REQUIRES	Assumptions that can be made by subprogram
TUNING	Relationship between values and performance

Software

Fast FFT code feeds DSP chip

Fast-Fourier-transform routine enables digital signal processor to invade array-processor territory

Long the domain of heavily funded projects using array processors, custom hardware, or superminicomputers, digital signal processing (DSP) has taken the first steps in migrating to low-end applications now that dedicated DSP microprocessors have arrived. And, with the introduction of a fast-Fourier-transform program and a separate DSP package, a Canadian firm specializing in digital signal-processing software is offering designers a chance to integrate high-performance DSP algorithms into systems employing one of these dedicated chips—the Texas Instruments TMS320 signal-processing chip.

DSP techniques, such as those for speech recognition, have relied heavily on frequency-spectrum analysis to extract distinctive features from input signals. In particular, the FFT has served as the cornerstone of DSP algorithms. With DSPS-2, Digital Signal Processing Software Inc. is teaming optimized software routines with the TMS320. Capable of performing a radix-4 64-point complex FFT in 600 µs, the package is already in use in the research-and-development laboratories of a Fortune 250 company, says L. Robert Morris, president of DSPS.

Competitive signal-processing microprocessors, such as the NEC µPD7720 and AMI S2811, manage only a 32-point complex FFT in 700 and 1,500 µs, respectively. "In fact," says Morris, "the execution time of the DSPS-2 FFT on the 320 is only about twice as slow as that of a $30,000-plus AP-120B array processor, which produces a 64-point complex transform in 280 µs."

Morris attributes the high speed attained with his package to special coding techniques that reduce overhead due to branch instructions (in-line coding) and coefficient address calculation (immediate addressing). Taking advantage of the large program address space and unique "multiply immediate" instruction of the TMS320, DSPS embedded the needed constants in the control code. In-line coding techniques, which aid elimination of branch instructions, result in position-independent code that may be loaded anywhere in off-chip memory without reassembly or modification. Thus the FFT routine can be placed in read-only memory.

Although DSPS exploited the large program space of the TI chip for this high-speed FFT, the firm expects to take advantage of another unique feature of the TMS320 for a future 256-point complex FFT package. Here, rather than placing executable instructions in line, a series of TMS320 computed–program-branch (CALA) instructions will cause execution to be threaded through common sections of code, thus reducing memory requirements.

Software designers will be able to utilize in-line coding through the use of a Macro-11-to-TMS320 cross-assembler from DSPS. With the cross-assembler, programs written on the PDP-11 from Digital Equipment Corp. are converted into in-line TMS320 machine code, which may then be loaded onto TI's TMS320 evaluation board through a serial interface.

Waste no time. Besides accompanying the FFT routine in the DSPS-2 product, the cross-assembler anchors another offering from DSPS, DSPS-3. With an eye on the emerging digital signal-processing market, DSPS brought together in DSPS-3 key concepts in time-efficient DSP software, producing a 500-page book and associated PDP-11 floppy disk. Along with the cross-assembler, the floppy disk carries the approximately 75 programs and program fragments written in Fortran, PDP-11 assembler, and TMS320 assembler that are described in the book.

DSPS-2 is available now for $1,500 (U. S.) and is distributed on a floppy disk for the PDP-11, containing the Macro-11-to-TMS320 cross-assembler and the TMS320 FFT supplied either in Macro-11 source form or as object code. Also available now, the DSPS-3 book and diskette with cross-assembler and programs is priced at $250.

Digital Signal Processing Software Inc., P. O. Box 5348, Station F, Ottawa, Ont. K2C 3J1, Canada. Phone (613) 231-7576 [371]

Logic language programs PLAs

Logic-equation compiler puts out fuse patterns for any type of field-programmable logic array

Calling field-programmable logic "the next really new technology for engineers," Assisted Technology Inc. has come up with a compiler that generates fuse patterns for any brand of programmable logic device when given logic equations written in a language called CUPL.

Programmable logic arrays are devices that can be customized by selectively blowing fuses in large arrays of gates, a process that achieves the economies of large-scale manufacturing while permitting the individual tailoring of devices. They differ from gate arrays in that PLAs are stockpiled after being fabricated up to the interconnect layer and then go through a final metalization step on customer demand.

PLAs come in several different architectures and with differing degrees of programmability. Manufacturers of each type of device provide their own unique progamming languages for the equations, which when downloaded to a programmer for programmable read-only memories, supply the proper interconnect patterns for the given PLA.

The Assisted Technology compiler, company president Robert Osann says, is the first that will operate with any kind of device; it contains device-desciption files that adapt the logic patterns to the pinout and internal architecture of each device. The programs will run on all popular PROM programmers, such as those from Data I/O, Stag, and Kontron.

CUPL (pronounced "couple"), the company's proprietary command language, is the first product of Assisted Technology, which Osann says was formed to develop software for PLA work. The language allows the programmer to group variables together in what the firm calls a macrovariable. Once defined, the macrovariable can be called with a single line of code so a line for each variable in the group need not be written.

The language's shorthand notation lets the user define several contiguous pin addresses by specifying the endpoints of the series of pins. The boundaries of a group of addresses that the PLA is to decode can be specified in a similar manner. Information headers give the designer space for complete functional descriptions of each section of code.

With CUPL, the chip designer can think in terms of logic, not gates, Osann says. The designer writes the Boolean equations, compiles them into a pattern that can be downloaded to a PROM programmmer, and blows the fuses. The connected chip can then be tested, and if it is in error, the designer can go back to the program and edit it. A logic simulator included in the package allows the user to verify logic equations.

Portable. The company has adapted CUPL initially to the IBM Personal Computer (with at least 128-K bytes of memory) on the grounds that it is the machine most widely available to engineers. The compiler, however, is written in C under Bell Laboratories' Unix and is highly portable, says Osann. Versions will be made available for VAX minicomputers and the 68000 microprocessor, and the language will eventually be adapted to gate-array work as well.

The Personal Computer version, including a full-screen editor (the programmer may use another editor if he or she chooses), will be available this month for $500.

Assisted Technology Inc., Suite 150, 2381 Zanker Rd., San Jose, Calif. 95131. Phone (408) 942-8787 [478]

IEEE floating-point math drifts to 8-bit chips

Supplementing its similar packages for the 8051, 8086, and 6809 microprocessors, U. S. Software now offers a pair of software libraries for floating-point mathematics operations on Z80- and 8085-based systems. The FPAC and DPAC libraries handle floating-point numbers in the format proposed by the Institute for Electrical and Electronics Engineers for single- and double-precision arthimetic, respectively. In addition to the standard arithmetic functions, the routines support trigonometric functions, conversion operations, and floating-point comparison functions that allow for small differences, or fuzz, between the operands.

Trimmable. Delivered in assembly-language source code, each library may be trimmed to support selected routine subsets. The Z80 single-precision FPAC routines occupy 3,600 bytes and the Z80 double-precision DPAC requires some 8,300 bytes in memory. Versions for the 8085 use 3,800 bytes for FPAC and 8,800 bytes for DPAC. On a 6-MHz Z80, FPAC routines perform 2,000 to 4,000 floating-point operations a second (flops), and DPAC manages 500 flops. Z-80 and 8085 FPAC and DPAC packages are available now, priced at $750 for FPAC and $1,250 for DPAC, which includes FPAC.

U. S. Software Corp., 5470 N. W. Innisbrook Place, Portland, Ore. 97229. Phone (503)-645-5043 [476]

32-bit systems target Ada work

Ada compiler and support tools run on Data General MV series and Rolm militarized versions

Ada, the high-level language mandated by the Department of Defense for use in the next generation of military software, is getting ready for the transition from its long development stage to wide-scale use. Therefore, with an eye toward defense contractors, which are expected to generate momentum in the market for Ada hardware and software tools, Data General Corp. says it will begin selling an Ada compiler and program-development and -transport package for its Eclipse MV 32-bit superminicomputer series.

Most customers for the Ada development package will be new to Data General equipment and in the market for a complete system, predicts Robert C. Miller, senior vice president for the firm's business divisions. Such systems will be based on the Eclipse MV/4000 with 4 megabytes of main memory and 147 or 277 megabytes of disk storage, the MV/8000 with 6 megabytes of main memory and 277 megabytes of disk, or the high-end MV/10000, which has 8 megabytes of main memory and a 554-megabyte disk capacity.

Prices for complete systems will range from about $147,500 up to $398,200. Depending on configuration, between 5 and 15 Ada programmers can be supported in completely dedicated systems; users, however may elect to add as options any of the family's full line of applications software. As the package is the result of a joint development and marketing effort with Rolm Corp., it will also available on Rolm's MSE/800 militarized versions of the Data General systems.

Logical layer. Fully compatible with the most recent Department of Defense and ANSI standards for the language (MIL-STD-1815 and ANSI 1815), the Rolm/DG Ada Development Environment package consists of a Kernel Ada Programming Support Environment (Kapse) that includes the required data base and that comprises a logical layer overlying the Eclipse MV's AOS/VS operating system, as well as software tools for program generation, debugging, and transport to target machines.

The utilities include a user interface with a help facility, libraries for such aids as basic language definitions and information about allowable operations or input/output capabilities, data-base control tools like a data-base manager and a mapper that guides library searches, application-program–development tools like an editor and debugger, and such target-development tools as the Ada compiler, target-code generators, and an object importer that brings into the Ada package binary modules produced by other compilers.

Faster. Despite the large complement of development tools available in the package, Data General will be working to expand the Ada development-tool kit and to optimize existing parts like the compiler and the debugger, says Miller. The compiler, which the company has tested using the Defense Department's validation test suite and which it hopes will receive validation by the Ada Joint Program Office by the time first deliveries start in fourth quarter 1983, now runs at 200 code lines per minute; Data General is aiming for eventual 600-line/min compilation.

The Ada Development Environment package will be demonstrated this month at the National Computer Conference in Anaheim, Calif.

Data General Corp., 4400 Computer Dr., Westboro, Mass. 01580. Phone (617) 366-8911 [372]

Rolm Corp., 4900 Old Ironsides Dr., Santa Clara, Calif. 95050. Phone (408) 988-2900 [439]

Real-time debugger bows in silicon

Designers can now develop embedded systems faster and more easily by using Tracer, a real-time software-debugging tool on a chip. Tracer performs with Hunter & Ready's VRTX operating system, a real-time multitasking silicon-software component for embedded systems.

Tracer and VRTX components support all custom and standard microprocessor boards and can be used with virtually any high-level language or development system. With Tracer, designers can obtain current system-state information and determine the status of application tasks in real time. In addition, the tool lets designers display the contents of the input/output buffer and examine or modify the contents of memory and registers at critical moments.

Tracer is available now with the company's VRTX R&D package, which includes a license to make five copies of the chip set for research and development use, and documentation. Tracer is also available as an option with VRTX, adding $650, when purchased for production use.

Hunter & Ready, 445 Sherman Ave., Palo Alto, Calif. 94306. Phone (415) 326-2950 [373]

Pack gives Personal Computer office-level word processing

A software package called NBI Word Processing, available immediately for the IBM Personal Computer, brings the professional-level word-processing features found on the company's OASys office-automation systems to personal computers. It also runs on the new IBM XT and the IBM-compatible Compaq portable computer. Documents created on the IBM Personal Computer can also be sent to OASys systems.

NBI Word Processing includes a coprocessor board, which is easily inserted into the Personal Computer. With 64-K bytes of memory and space to allow memory expansion in 64-K-byte increments up to a maximum of 192-K bytes, the coprocessor board also provides memory expansion for other computing tasks.

Functions fulfilled by the software include form letters, printing while editing, automatic centering, disk password security, and a typewriter mode for line-by-line printing for forms and envelopes. In addition, in-depth user-assistance menus at three increasing levels of detail are provided. The suggested retail price is $695.

NBI Inc., P. O. Box 9001, Boulder, Colo. 80301. Phone (303) 938-2795 [375]

Lisp option gives computer line artificial-intelligence capabilities

The Lisp artificial-intelligence programming language is now available for Cromemco's complete line of 8-, 16-, and 32-bit computer systems. Lisp is designed for use in such data-base applications as systems that understand natural language, systems for symbolic manipulation of mathematical expressions, intelligent controllers, robotics, computer-aided design, and design automation.

Key to these applications is the use of Lisp to develop what are called expert systems that emulate the way people think. Unlike algorithmic programs in conventional computers, expert systems do not operate according to specific, set decision paths. Instead, they can weigh facts and make appropriate choices for each problem.

Cromemco's Lisp incorporates features like standard control constructs, fixed and floating-point arithmetic, an extensive utility library, and the ability to interface with non-Lisp procedures.

Available for any System One, Two, or Three, Lisp is priced at $595. It is delivered on either a 5¼- or 8-in. disk.

Cromemco Inc., 280 Bernardo Ave., Mountain View, Calif. 94043. Phone (415) 964-7400 [374]

Firmware generator writes operating systems in silicon

A firmware-generator version of MTOS-68K, a real-time multitasking multiprocessor operating system for

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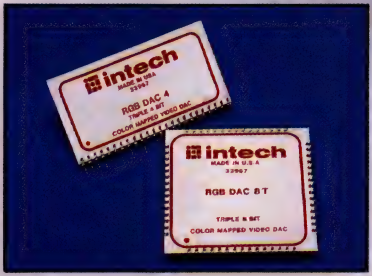

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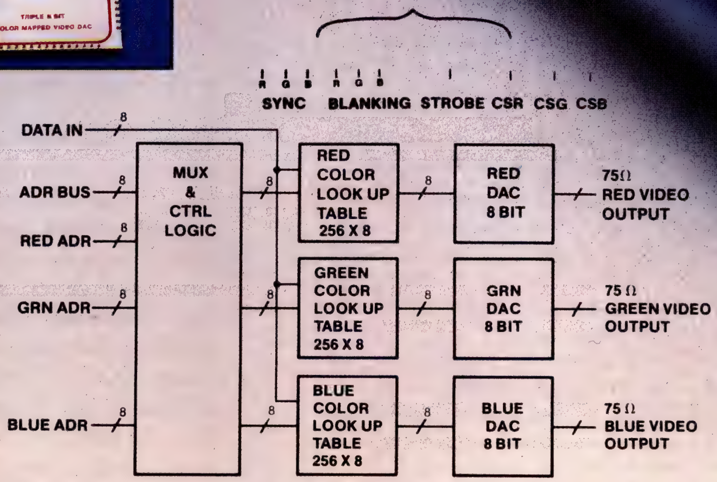

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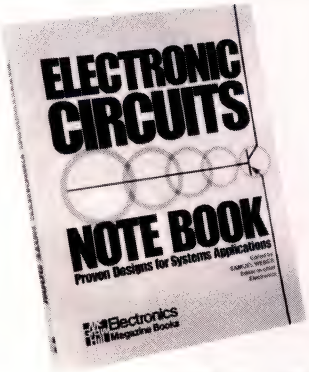

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the 68000, is provided in source language and facilitates the customized production of silicon operating systems. Called MTOS-68KFG, it is configurable by the user as firmware for a variety of available single-board computers, as well as for unique board configurations.

All of the facilities of MTOS-68K, such as support for multiple processors, priority scheduling, and task, time, and interrupt management, are available to the user of MTOS-68KFG. The basic package contains the MTOS-68K executive, a dynamic debugger, a console driver, and a test program. An optional monitor may be used to download application software as well as to provide hardware-oriented debugging capabilities.

MTOS-68KFG is sold for $11,000, with a liberal licensing policy that entitles the purchaser to embed the object program in products without further charges.

Industrial Programming Inc., 100 Jericho Quadrangle, Jericho, N. Y. 11753. Phone (516) 938-6600 [376]

Finite-element program runs on Perkin-Elmer minicomputers

Thanks to a joint development effort with Swanson Analysis Systems, the latest version of Ansys, a large-scale, general-purpose finite-element computer program, is available on Perkin-Elmer series 3200 minicomputers. Previously available only on mainframe computers, Ansys boasts linear and nonlinear capabilities in structural and heat-transfer analysis to solve problems in the communications, automotive, aerospace, and electrical industries and the like.

Ansys can be run in either an interactive or a batch mode. When it is running interactively, the user can take advantage of program-contained documentation, immediate graphics display, and options to correct input errors. Analysis can be done efficiently by creating the model interactively, obtaining the solutions in a batch mode, and interpreting the results interactively.

With Ansys, users can simulate both two- and three-dimensional models. Users can subject a model to loads like temperature or seismic forces, pressure, or friction and study the resulting stress in detail.

Depending on which series 3200 computer Ansys is mounted, it is priced from $1,500 to $2,500.

Perkin-Elmer Corp., Data Systems Group, 2 Crescent Place, Oceanport, N. J. 07757. Phone (201) 870-4768 [377]

Swanson Analysis Systems Inc., P. O. Box 65, Houston, Pa. 15342. Phone (412) 746-3304 [378]

Data-base manager handles CMS, DOS operating systems

The model 204 data-base management system, previously available only to organizations running OS, has been extended to the CMS and DOS operating systems. Also, the company has introduced a document-handling subsystem. Full-screen editing has been added free of charge.

The CMS version has been implemented in both single- and multiple-user configurations. The multiuser version allows large numbers of users to concurrently access and update data bases under the control of a model 204 virtual machine, with very little performance degradation. The CMS version, available in June, will sell for $195,000.

Model 204 is appropriate for the DOS environment because it works with all IBM teleprocesssing access methods. Consequently, users can develop on-line applications without the costly overhead in system programming, application programming, and machine resources of a teleprocessing monitor. Available now, the DOS version goes for $155,000.

Text/204, an integrated model 204 subsystem, is an on-line document-storage and -retrieval system. It manages large numbers of documents, modifies stored documents on line, and dynamically updates all keyword indexes. This $30,000 option is available now.

Computer Corp. of America, 4 Cambridge Center, Cambridge, Mass. 02142. Phone (617) 492-8860 [379]

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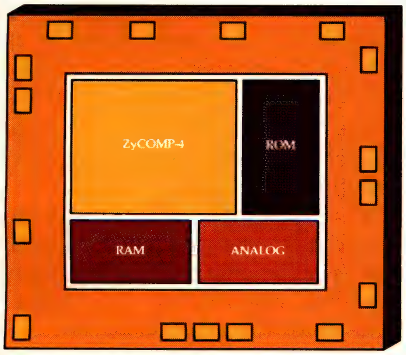

The ZyCOMP-4, a complex standard cell, is a 4-bit core processor that can be combined with other standard cells (RAM, ROM, I/O, etc.) to create a customized microcomputer chip. It can be architecturally mapped to 6502 or 8049 processors, providing the best features of both.

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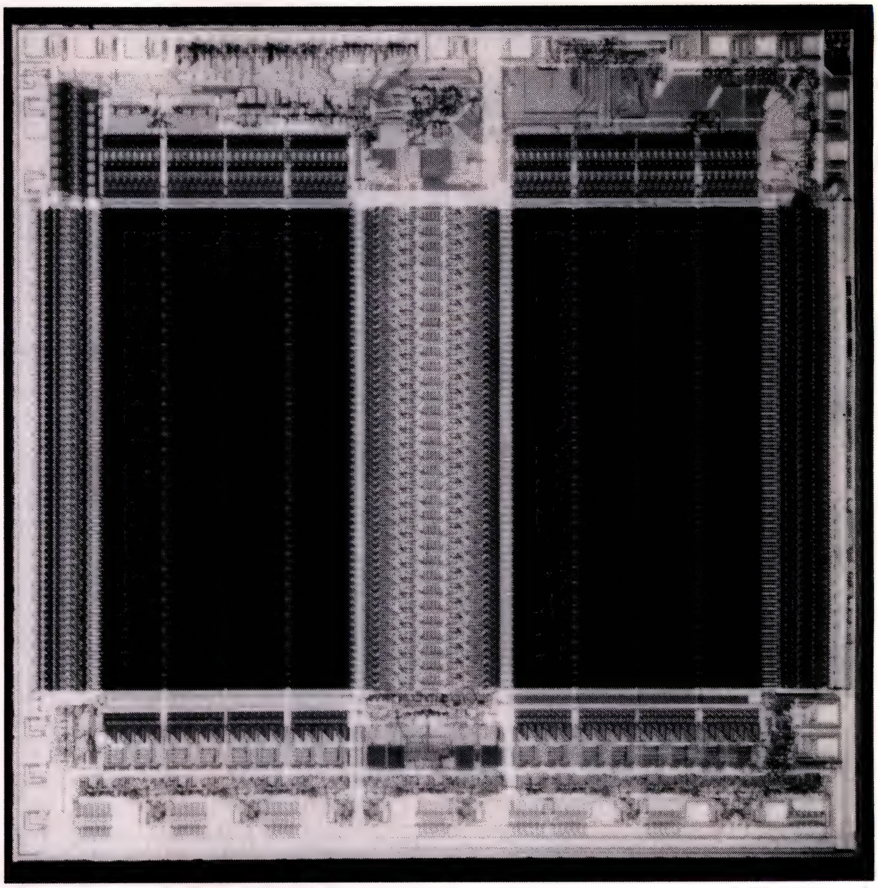


At least a half dozen chip makers have announced plans to pursue the emerging market for dense, easy-to-use electrically erasable programmable read-only memory devices. With the introduction of a 32-K part having 5-V–only operation, byte-wide organization, and a number of convenience features, NCR Corp.'s Microelectronics division confirms its intention to be a force in this market.

Known as the NCR 52832, the 4-K-by-8-bit EE-PROM is fabricated using the same n-channel double-polysilicon SNOS (silicon nitride oxide silicon) process employed in NCR's family of 5-V–only byte-wide nonvolatile random-access memories—RAM arrays shadowed bit for bit by on-chip EE-PROM cells—brought out earlier this year [*Electronics*, Jan. 27, p. 128]. Like those devices and the 256-bit NCR 52801 EE-PROM, the 52832 employs an on-chip substrate bias pump to generate the necessary program and erase voltages from a 5-V supply.

Though such suppliers as Seeq Technology Inc., Inmos Corp., and Xicor Inc. have announced plans to produce 64-K EE-PROMs, NCR officials expect that timely availability of the 52832 will ensure a market for the part. The device will be available in sample quantities this month with production of commercial-grade parts set to begin in July. "We expect to be in production on this part for at least a quarter before the 64-K parts [announced by competitors] hit production," says Walter Krysiak, NCR's applications and strategy manager for nonvolatile memory. Such a lead will enable the firm to "get down the learning curve and offer significant cost-per-bit advantages" compared with competitors' 64-K parts, he believes. NCR plans to offer samples of its own 64-K EE-PROM by the fourth quarter.

In 100-piece quantities, the TTL-compatible 52832 will be priced initially at $39.62 each for commercial-grade parts in a 28-pin plastic dual in-line package. The pinout used follows a proposed standard not yet fully approved by the Joint Electron Device Engineering Council.

The device will also be offered in a 28-pin ceramic DIP and in a 32-terminal Jedec type E leadless chip-carrier, though pricing on these versions has not yet been set. The 52832 will be offered for use in three operating temperature ranges (0° to 70°, –40° to 85°, and –55° to 125°C), with military-grade parts to be available in production quantities beginning in the fourth quarter.

With access times to be specified at 200 ns typical and 300 ns maximum for commercial-grade parts, the 52832 will be fast enough for use with many microprocessors. On-chip latching of addresses and data will also free the processor during the part's 10-ms write cycle.

Foremost among the 52832's user-convenience features is a page-write mode not offered on currently available competitive EE-PROM parts, says Thomas J. Tyson, NCR applications engineer. Using this feature, data can be loaded into the part and latched either 1 byte at a time or in multiple bytes up to a maximum of 16 bytes (one page) for writing in one 10-ms cycle, enabling the entire 32-K part to be written in less than 3 s. This is more than an order of magnitude improvement over competitive byte-alterable devices with 10-ms write cycles, which require about 40 s to write, Tyson points out. The feature also saves money by reducing device test times, he adds.

Checks margins. Another feature believed to be unique for an EE-PROM is on-chip memory-margining circuitry, which allows data-retention time and the number of write or erase cycles possible to be characterized by measuring written voltage levels in the device cells. This will be used by NCR to improve reliability. It may also be used by the customer to measure at any time the remaining data-retention capacity of a device (which degrades as a function of time, temperature, and endurance cycling). Unlike 52832 operational modes, however, additional +22- and –5-V supplies are required to use the margining feature.

NCR guarantees 52832 data retention—over the full military temperature range of the part—of 10 years with 10^4 write-erase cycles using a 10-ms write time. And for customers who want it, the firm will investigate the possibility of a larger number of write-erase cycles with a shorter data-retention guarantee. Though characterization is not yet complete, indications are that 10^5 write-erase cycles with one-year data retention may be possible, Tyson says.

Endurance. Competitors' claims to the contrary, Tyson says that the nitride oxide nonvolatile storage approach used by NCR and others including General Instrument Corp. has potential for endurance equal to that of floating-gate nonvolatile storage technologies used by Seeq, Xicor, Inmos, and Intel Corp. Test chips fabricated in NCR's SNOS process have exhibited sufficient data retention after more than 10^7 write-erase cycles, NCR officials say.

The 52832 can be erased by page (any contiguous 16 bytes specified by the user) or in a block (entire chip) mode. Unlike some competitive chips, which require higher voltages for a block erase, the 52832 requires only 5 V for either erase mode, Tyson notes. Power dissipation on the part will be about 160 mW active and about 80 mW standby. Maximum power dissipation will be specified after more data is available but is expected to be less than 350 mW active.

The device will be fabricated using 4-μm minimum channel geometries, producing a die of about 40,000 mil^2. Plans call for scaling to either 3- or 3.5-μm minimum geometries by the first half of next year, says Krysiak. The 52832 will be pin-compatible with NCR's planned 64-K EE-PROM. NCR does not now plan to produce a 16-K EE-PROM device.

NCR Microelectronics Division, Product Marketing, 8181 Byers Rd., Miamisburg, Ohio 45342. Phone (800) 543-5618 or (513) 866-7217 [411]

Chip enhances low-cost radios

Producing pseudo-stereo output from mono input, device makes speakers sound widely spaced

Following hard on the heels of its TDA7000 single-chip frequency-modulation receiver [*Electronics*, Jan. 27, p. 129], the Philips Electronic Components and Materials (Elcoma) division is introducing what it claims is another first in the audio field—a circuit that integrates all components for pseudo-stereo and spatial-stereo effects on a 6.5-mm^2 chip.

In the TDA3810, the pseudo-stereo circuitry splits and routes the incoming mono signal into two channels. One channel goes straight to the output, while the other channel imparts a delay of about 500 μs to all frequencies above 300 Hz. The channel separation is around 55 dB. The result resembles stereo sound.

The signals below 300 Hz, the unaltered signals, in effect fill out the sound between the speakers. In other words, the bass instruments sound as if they are coming from everywhere, not from individual speakers.

"This stereo effect is subjective, of course," says Peter Langendam, product marketing manager at Elcoma's Valvo facilities in Hamburg, West Germany, where the device was designed and will be fabricated. "So we have kept low-pass filters off the chip to allow set makers to customize their circuits for the best possible pseudo-stereo sound."

The spatial-stereo effect is achieved by using two on-chip operational amplifiers in the signal path of each channel. Each op amp has its own feedback resistor connected to its input. The ratio of the two resistance values determines the anti-phase crosstalk between the channels. This crosstalk, about 50%, gives the impression of a greater distance between the speakers.

In addition to these effects, the 3810's designers aimed to keep the signal-to-noise ratio and harmonic distortion to as low a level as possible. The signal-to-noise ratio checks in at 80 dB, and tests of the first samples have shown the harmonic

Pseudo, spatial stereo suit portable radios

With the relatively wide availability of true stereo broadcasts, the usefulness of such a chip as Philips' TDA3810, which can produce both pseudo- and spatial-stereo effects, is not immediately obvious. The designers at the firm's Elcoma division see one prime market for such devices in low-cost two-speaker radios, including car radios, where the device will produce stereo-like effects without expensive stereo decoder circuits. Another is in portable stereo radios and television receivers, where the chip's full range of features can be exploited.

Although stereo broadcasts are common for fm programs, most music programs on ordinary radio and television are transmitted in monaural sound. Pseudo-stereo circuits, until now in discrete form, process a monaural signal in such a way that the output has an almost realistic stereo effect, one that the firm says is difficult to distinguish from real stereo. Likewise, for weak fm stereo signals the pseudo-stereo circuits can take over and produce stereo-like sound without the hiss that can plague diminished stereo reception.

For a radio or TV set with stereo decoding, the TDA3810 can be used to produce pseudo-stereo sound when a monaural signal is being received. If the transmitter puts out a stereo signal, the pilot tone accompanying that signal activates the set's stereo decoder, which in turn switches the 3810 to the spatial-stereo mode. The latter is of advantage in sets where both speakers are in a single cabinet and thus are fairly close together: the listener is given the impression that the speakers are widely spaced, as they normally are for high-fidelity stereo systems.

distortion to be between –80 and –90 dB. One potential user, Langendam says, reported that the distortion was so low that his test gear was not sensitive enough to measure it.

Quiet switching. Another design target was noise-free switching within the device. Switching noise has been a problem for designers of similar circuits made with discrete components, particularly when weak signals are encountered. With noise-free switching, the receiver can alternate between stereo and mono as the signal goes above and below the threshold needed for stereo.

The Valvo engineers have eliminated switching noise by integrating fast muting circuitry. And noise occurring when the IC switches automatically from mono to pseudo or spatial stereo is made inaudible by on-chip input-current compensation.

The 3810 has outputs that directly drive light-emitting diodes to indicate spatial stereo or pseudo stereo. It operates off supplies of between 4.5 and 16 V and is encapsulated in an 18-pin SOT-102 dual in-line package.

Samples of the 3810 are available now, with volume production expected by early June. It will sell for about $1.50 each, with discounts in lots above 10,000 pieces.

Signetics Corp., 811 East Arques Ave., P. O. Box 409, Sunnyvale, Calif. 94086 [479]
Philips Electronic Components and Material Division, Hurkse Street, 5600 Eindhoven, The Netherlands [480]

Digital driver protects outputs

Quad-output device shuts down overloaded line while letting other three continue operation

Power drivers, or peripheral drivers as they are sometimes called, are popular chips for driving anything from relays and stepper motors to high-current light-emitting diodes for fiber-optic communications. These drivers, which accept TTL or MOS logic inputs (on the order of 1 μA, typically) and supply from 250 to 600 mA of output, come with two or four outputs per package. The trouble with existing devices is that if there is a problem with one output—such as a stepper motor stalling or an output shorted to the supply—all the outputs turn off.

A peripheral driver from National Semiconductor Corp. solves this problem with unique output-protection circuits. These circuits shut down a given output if it exceeds a preset current limit, allowing the other outputs to function normally.

Called the DS3668, the driver is a quad-output device that is pin-compatible with the Texas Instruments SN75437. Each of the four outputs is capable of sinking 600 mA to ground, but if any output exceeds 1 A for more that 25 μs, typically, the protection circuit shuts it down. The 25-μs delay ensures that the protection circuit is not triggered by surge currents generated when capacitive loads are turned on.

No latchup. Each output is an open-collector transistor with a breakdown voltage of 70 V and the ability to sink 600 mA. For inductive loads, on-chip clamping diodes limit the fly-back voltage to 35 V, eliminating latchup during turn-off. In addition, the DS3668 incorporates circuitry that guarantees glitch-free power-up and -down. A fail-safe feature is designed to put the outputs in a high-impedance state when an input is open.

A special copper leadframe was developed to increase the allowable power dissipation to 2 W from the 1 W normal for a 16-pin plastic dual in-line package. All four ground pins on the chip are directly connected to the new frame. When the DS3668 is soldered onto a printed-circuit board, the power rating is further increased.

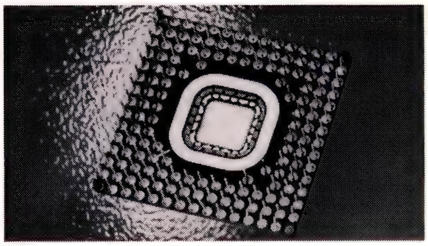
The DS3668 peripheral driver is available now and is priced at $5.40 each in quantities of 100.

National Semiconductor Corp, 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-4095 [412]

2,800-gate, TTL-compatible part added to Macrocell library

The latest item in the Macrocell array library is a TTL-compatible part, the MCA2800ALS, that has a comlexity of 2,800 equivalent gates and a gate propagation delay of 600 ps. Macrocell arrays differ from conventional gate arrays in that the complex large- and very large-scale integrated functions are developed not from the interconnection of simple gates, but rather from a library of more sophisticated circuits (or macros) including flip-flops, decoders, and multiplexers.

The MCA2800ALS comprises 130 internal cells. Each cell may be personalized through a computer either as simple OR or NOR gates (up to four per cell) or as more complex functions, such as a full adder (two per cell). Combinations of simple and complex macros within a single cell are allowed.



There are, in addition, 120 input/output cells that may be personalized as off-chip drivers, off-chip receivers, or bidirectional I/O cells with three-state or open-collector or active pull-up outputs. Typical receiver delay is 1 ns. The output driver can sink 12 mA and has a typical delay of 5 ns with a 50-pF load.

The arrays are housed in 149-pin ceramic bed-of-nails pin-grid–array packages. Development cost of the first design is $25,000. This includes computer-aided–design training, access to Motorola's CAD system, 10 tested prototypes, and automatic test-program generation. Pricing, in lots of 500, is about $160 each.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 962-2516 [413]

Memory interface chips serve multiplexed bus at 5 MHz

Capable of interfacing directly with CDP1800-series complementary-MOS microprocessors, a family of C-MOS 6-bit latch and decoder memory interface chips called the CDP1881/1882 series operate on a CDP1800's multiplexed address bus at its maximum clock frequency of 5 MHz.

The 1881 and 1882 operate with both 2-K- and 4-K-byte memories. For example, they can interface with up to four 4-K-by-8-bit read-only memories to decode a 16-K-byte ROM system or with up to four 2-K-by-8-bit random-access memories to decode an 8-K-byte RAM system. Output drive capability is one TTL load, for use with n-channel MOS as well as C-MOS RAMs and ROMs.

In quantities of 100 pieces, prices range from $1.64 for a 5-V CDP1882 to $2.85 for a 10-V CDP1881. Parts are available now.

RCA Solid State Division, Rte. 202, Somerville, N. J. 08876. Phone (201) 685-6423 [415]

256-K memory array provides configuration flexibility

Because it contains four 16-K-by-4-bit memory chips, each with its own unique chip-select line, the 256-K DP256U static complementary-MOS random-access-memory hybrid circuit may be organized as 64-K by 4 bits, 32-K by 8 bits, or 16-K by 16 bits. Operable off a single 5-V power supply, the part consumes just 400 mW in active mode; it takes only 64 μW to retain data.

Access and cycle times are identical, with versions offered that at 75, 90, and 105 ns. The DP256U may be ordered in commercial, industrial, or military grades.

Available now, parts range in price from $1,200 for commercial parts to $1,500 for the military versions.

Dense Pac Development Ltd., 18612 Minuet Ln., Anaheim, Calif. 92807. Phone (714) 779-7123 [417]

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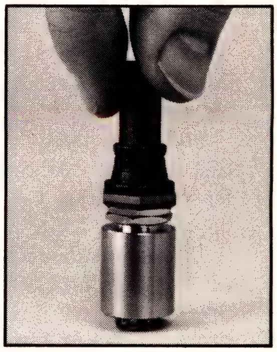

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Circle 166 on reader service card

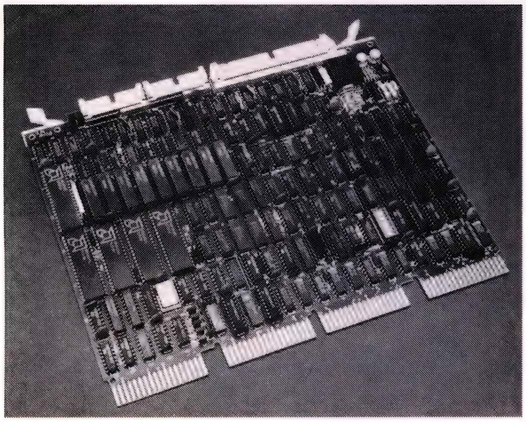
Computers & peripherals

Boards control mix of drives

Flexible controllers handle variety of tape and disk drives for Q-bus and Unibus computers

Aiming at a consolidation of its position in the market for peripheral controllers for Q-bus– and Unibus–based computers from Digital Equipment Corp., MDB Systems Inc. is introducing controller cards for a variety of disk and tape drives. The controllers are designed to interface with up to four drives, handling a mixture of drive types and modes of operation.

The TM-11–compatible tape-drive controllers, one a quad-width board for Q-bus systems and the other a hex-width unit for the Unibus, are software-configurable. Driver configurations can be changed or added without powering down the system and resetting switches on the controller board, which is the usual method.



Setup saved. From the console, the operator can modify the controller's addressing, bus levels, and numbers, as well as its parameters, priority interrupts, and and vectoring for each attached tape drive. The configuration is stored in nonvolatile random-access memory and can be saved for use at the next system power-up. On-board firmware includes extensive self-testing routines that are executed upon system power-up.

Up to four tape drives can be controlled by a single card, and they can operate at any combination of tape speeds, using either phase-encoded or inverted–nonreturn-to-zero recording standards. The controllers have embedded formatters, eliminating the need for individual external formatters for the attached tape drives.

The MLSI-TM11 tape-drive controller for the Q-bus is priced at $2,600 in single units. The Unibus model, designated MDB-TM11, sells for $2,950. Both will be available in production volumes by August.

The company's new line of disk-drive controllers includes models that emulate DEC's RM02, RM03, and RM05 storage-module drives, as well as versions that emulate the RK06 and RK07 drives. Most of the controllers are quad-width cards able to handle two drives at a time, but one hex-width model, the MDB-RM11H, can support up to four RM-series drives.

The MDB units can simultaneously control any combination of two fixed or removable disk drives using any of the emulation modes offered. The capacity of up to 512 megabytes per formatted drive will increase along with disk technology, according to the firm.

The disk controllers are compatible with the driver and diagnostic routines of all DEC operating systems (as are the tape controllers), as well as with Unix and other operating systems, with no modification necessary. Media compatibility is maintained with the RM-series drives; a disk pack can be switched from a Control Data Corp. storage module drive to a DEC drive, thanks to the formatting of the MDB controller.

The disk units make use of a DEC-compatible 32-bit error-checking and -correcting code, a cyclic redundancy checking scheme with a 16-bit header, and media-defect flagging. Multiple sectors are buffered to eliminate late-data errors, and a direct-memory-access throttle feature transfers data in bursts of 1 to 16 words.

After interrogating a switch for data on the disk-drive types in use, the controller automatically structures its firmware to identify drives by the number of cylinders, sectors, heads, and blocks in each logical unit (one drive can be divided into a number of logical units). Four-level priority and interrupt vectors are selectable. As with the tape units, the disk controllers are compatible with 16-, 18-, and 22-bit address buses.

Emulating RK-series drives, the MDB-RK11Q quad-width controller is priced at $2,800 in single units. The MDB-RM11Q for RM-series disk drives sells for $3,200, and the hex-width, four-drive MDB-RM11H is $3,500. For Q-bus–based systems, the MLSI-RM11 and -RK11 are priced at $2,800 and $2,200, respectively. These disk-drive controllers are available now.

MDB Systems Inc., 1995 North Batavia St., Orange, Calif. Phone (714) 998-6900 [361]

Bubble-memory cartridge serves three systems

A removable bubble-memory cartridge offered in several data capacities can be used with any of the three bubble-memory systems becoming available from Targa Electronics Systems Inc. Cartridges initially will have capacities of 128-K and 256-K bytes and operate over either a 0°-to-55°C or 10°-to-40°C temperature range. Later, the firm expects to have 1-megabyte cartridges with extended temperature ranges.

The top of the line is the DR3101 data recorder, a peripheral device that emulates a tape or disk drive. The unit includes both RS-232-C and IEEE-488 communication ports, with software implemented to emulate a Digital Equipment Corp. TU-58 tape-cartridge recorder and a Hewlett-Packard floppy-disk drive. With the RS-232-C interface, communication with the host is handled at speeds up to 38,400 b/s.

For those applications where a floppy-disk drive would be ideal but the environment involves too much dust, vibration, or shock, a floppy-

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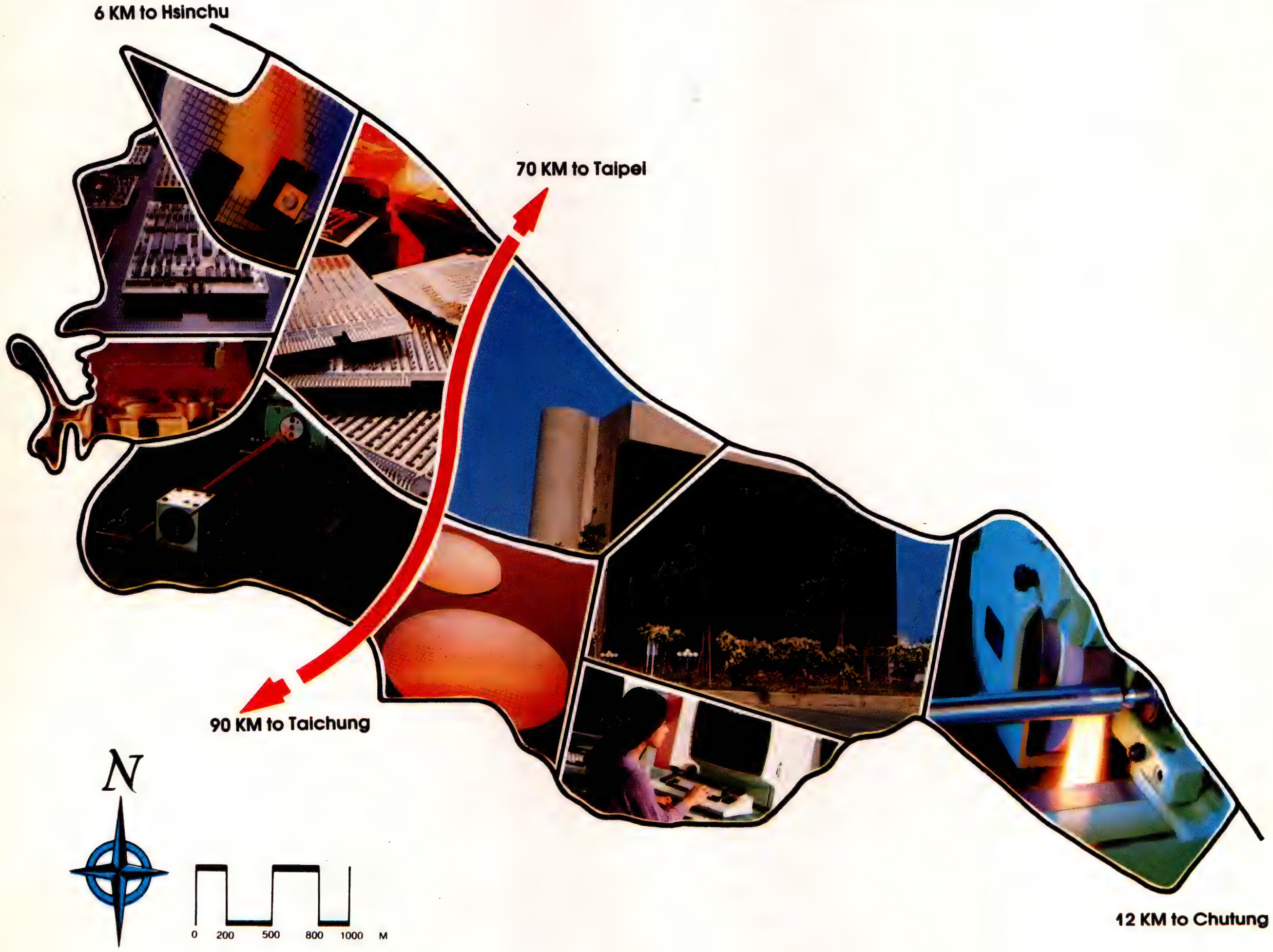

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disk emulator called Solidrive FDE525 fits the bill. The system is electronically compatible with American National Standards Institute standard 5¼- and 8-in. floppy-disk drives and fits the 5¼-in. footprint.

The third system is a subassembly for original-equipment manufacturers called the CH2100 cartridge holder interface. With the CH2100, manufacturers of portable computers, data-acquisition systems, process-control equipment, and many other instruments and peripherals can take advantage of the ruggedness of bubble memory at a reasonable price.

Systems range in price from $2,175 to $7,437.

Targa Electronics Systems Inc., P. O. Box 8485, 3101B Hawthorne Rd., Ottawa, Canada K1G 3H9. Phone (613) 731-9941 [363]

Supermicrocomputer gets a Unix-based network

By implementing a Unix-based Network Operating System (NOS) and a Unix System III Virtual Protocol Machine (VPM), Plexus Computers Inc. has brought extensive networking and mainframe communications capabilities to its family of 16-bit Unix-based supermicrocomputers.

NOS, which employs Ethernet hardware, not only enables the Plexus family of computers to communicate over a local network, but also supports a building-block approach that lets users erect a network of systems that collectively can outstrip the capabilities of traditional minicomputer systems. NOS, available in July, sells for $1,500 for each Plexus system. A complete Ethernet hardware kit lists for $3,450.

The company claims to be the first to implement VPM under Bell Laboratories' Unix. A high-performance data-communication subsystem of the Unix System III operating system, VPM enables users to link Plexus 16/32- and 16-bit supermicrocomputers to mainframes from IBM and other suppliers.

VPM, available now, is automatically included in the Plexus implementation of the Unix System III operating system. Remote–job-entry (RJE) applications are also supported under VPM. RJE uses the Hasp multileaving work-station protocol. Jobs submitted to a mainframe for processing under RJE return to the Plexus system, where they can be printed, stored , edited, or processed further by Unix-based software. RJE goes for $750 and is available now.

Plexus Computers Inc., 2230 Martin Ave., Santa Clara, Calif. 95050. Phone (408) 988-1755 [364]

Fiber-optic terminal serves TI's business systems

Users of Texas Instruments' Business System 600- and 800-series computers can replace their 911 or 940 terminals with a model that offers fiber-optic transmission or Electronic Industries Association (EIA) standard RS-232-C communications. The fiber-optic version for local links up to 3,000 ft long provides immunity to electrical noise and transmission rates of up to 19.2 kb/s.

The other version offers an RS-232-C port for short-distance connections or remote connections through a modem. The terminal has an auxiliary port for driving a printer. Print buffers let the operator use the terminal while a print operation executes.

The terminal has a green-phosphor screen and a 128-character ASCII keyboard, plus a 10-key numeric keypad and 12 function keys. The screen can display 24 lines of 80 characters each; a 25th line is used for status messages. Available in September, the terminal ranges in price from $1,295 to $1,450.

Also to be available in September are two interfaces for use with the 600- and 800-series computers. The communications interface CI404 provides four fiber-optic channels for conection to four model 931 terminals. The CI403 provides four buffered asynchronous channels to support the EIA version. The CI404 goes for $1,500, the CI403 for $1,100.

Texas Instruments Inc., Data Systems Group, P. O. Box 402430, H-650, Dallas, Texas 75240 [365]

Unit lets 3278 terminals run 8- and 16-bit software locally

A dual-processor system can transform virtually all asynchronous and IBM 3278–class terminals into intelligent work stations offering both CP/M and MS-DOS personal-computing capabilities. The Avatar TC100 runs all standard CP/M, CP/M-86, and MS-DOS software.

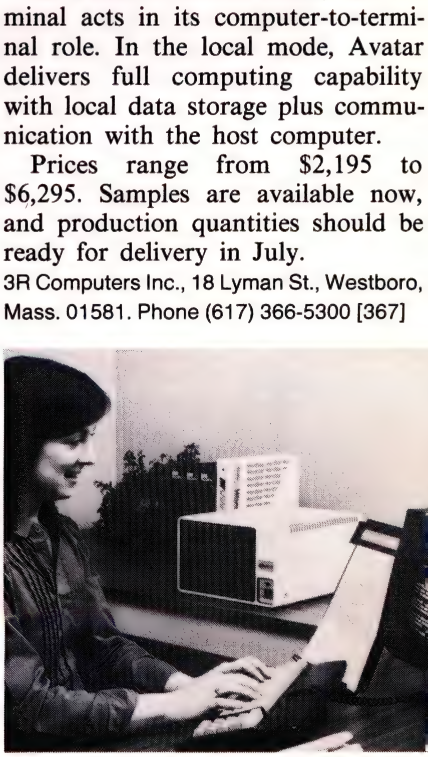
The TC100 features a single-board shared-memory architecture with both Z80 and 8088 microprocessors and 128-K bytes of dynamic RAM, expandable to 256-K bytes. The TC100's 8088 runs at 8 MHz, considerably faster than the one in the IBM Personal Computer.

The TC100 also includes ports for connection to host computers, local printers, corporate and public data bases, as well as communication and software utilities like those for file and data transfer. The system is available with either single or dual 5¼-in. floppy-disk drives for up to 1.6 megabytes of storage or an integrated Winchester and floppy system with up to 21 megabytes.

In Avatar's on-line mode, the terminal acts in its computer-to-terminal role. In the local mode, Avatar delivers full computing capability with local data storage plus communication with the host computer.

Prices range from $2,195 to $6,295. Samples are available now, and production quantities should be ready for delivery in July.

3R Computers Inc., 18 Lyman St., Westboro, Mass. 01581. Phone (617) 366-5300 [367]



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Data acquisition

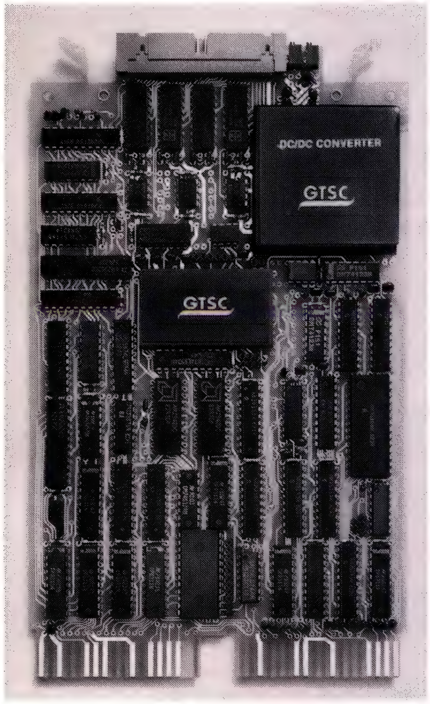
200-kHz analog card fits Q bus

12-bit, 16-channel analog-input subsystem for LSI-11 offers high speed without high price

A popular, if not ubiquitous, tool in laboratory and other measurement applications, Digital Equipment Corp.'s LSI-11 series of microprocessor-based systems gets a boost in its data-acquisition capabilities with Grant Technology Systems Corp.'s model 122 analog-input board.

Using a direct-memory-access interface to the LSI-11 family's Q bus, the 122 transfers data into system memory at up to 200 kHz. This is better than 60% faster than any comparable subsystem available, yet at $1,795, the unit sells for about the same as its nearest competitors, says GTSC president A. L. Grant.

Two similar GTSC boards, the $1,295 model 120 and the $1,495 model 121, yield maximum data rates to memory of 50 and 150 kHz, respectively. All three models, built on standard DEC dual-height printed-circuit boards, normally handle 16 input lines, although a $150 expansion option doubles that capacity.



Users may configure the full number of input lines three different ways with jumpers. They may be set up as single-ended channels or as pseudodifferential channels (all lines referenced to a common ground through one input to an on-board multiplexer and differential amplifier). The third option is configuration of the input lines as 8 or, with the expansion option, 16 differential-input channels using both available inputs of the board's multiplexer and differential amplifier.

Jumpers also select one of three input-signal ranges for the 122 and its companion boards: 0 to 10, –5 to +5, and –10 to +10 V. The board contains overvoltage protection circuitry, which ensures continued operation at up to 5.6 V over a normal 10-V input and protects the board from damage at power-down.

Inputs to the board pass through the multiplexer and differential amplifier to a high-speed sample-and-hold unit and on to the board's 12-bit analog-to-digital converter, which performs conversions in 3 μs with maximum linearity error of ±0.01% of full scale. A buffer register holds the digitized data for transfer to the host microprocessor, memory, or system peripherals.

Acquisition modes. The boards' three control registers accommodate user programming for several modes by which the boards gather data and direct it into the LSI-11 system's memory. The boards may operate in an automatically triggered channel-scanning mode over a specified number of input channels, continuously address one channel in the static mode, or respond to an external trigger in accessing input channels.

For DMA data transfers, users may move up to 64-K words into any selected portion of the LSI-11 address space. The boards have full 22-bit addressing capability, which lets them make use of the extended address space of the high-end LSI-11/23 Plus system.

The GTSC boards' control registers also permit programming of input and output, including setting interrupt priorities that take advantage of the LSI-11's four-level interrupt structure. The boards further contain an output for calibration and self-testing, letting the user dedicate one or more channels to automatic self-test routines. Four interrupt vectors also flag errors in the data-conversion sequence.

The models 120, 121, and 122 analog-input subsystems, available with original-equipment-manufacturer discounts of up to 35%, are deliverable from stock to 60 days.

Grant Technology Systems Corp., 11 Summer St., Chelmsford, Mass. 01824. Phone (617) 256-8881 [381]

Acquisition system is accurate to 16 bits, runs under Fortran

Designed for scientific and industrial data-acquisition applications requiring a fully integrated system, the Focus 5000 series of data-acquisition and -control systems operates at up to 100,000 measurements/s at an accuracy of up to 16 bits. It also has the flexibility to support in excess of 1,000 channels of analog and digital input/output.

The Focus systems, programmable in Fortran, acquire, condition, process, and transmit a wide variety of signal types within a mobile Retma enclosure. They can be configured from over 85 analog and digital I/O boards varying from simple multiplexers to completely isolated low-level input units, permitting direct implementation in many applications. Focus is designed to maintain laboratory-grade performance even in difficult environments.

The Focus 5010 version runs under the RT-11 operating system optimized for single-user access; the Focus 5020 operates under RSX-11M for multiuser multitasking operation. Both models provide 128-K bytes of random-access memory and 30 megabytes of mass storage on a Winchester disk drive.

Available now, the systems are

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For more information,
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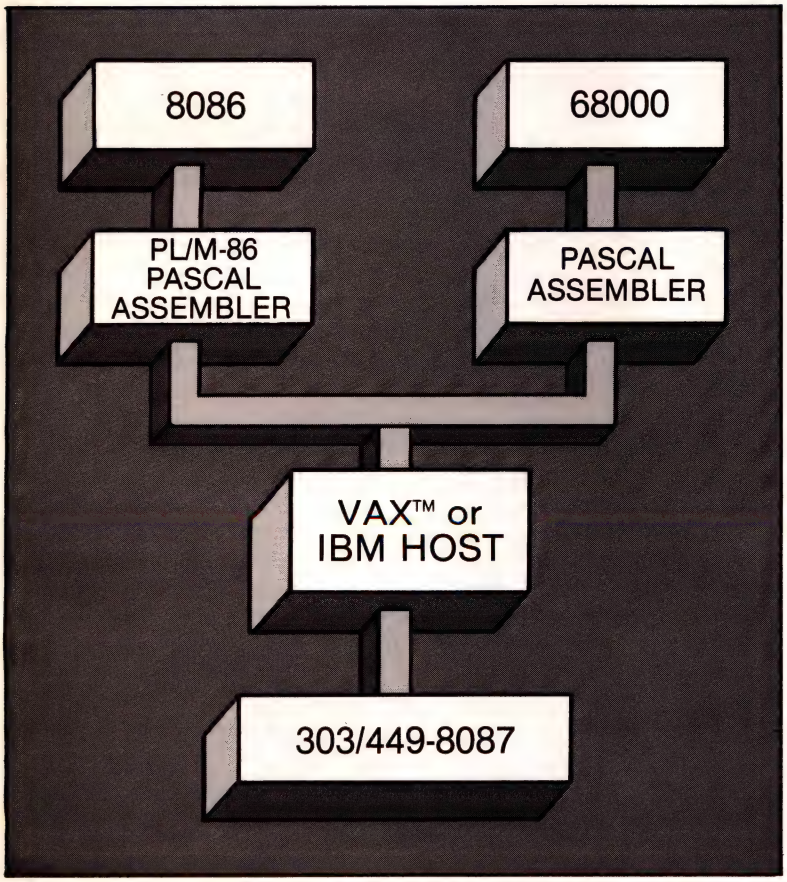
Circle 173 on reader service card



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XDS-86 additionally features a PL/M-86 language compiler and ICE-86™ debugger support.

XDS-86 produces Intel-compatible object formats, while PAS-68 produces Motorola S-records.

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4885 Riverbend Rd., Boulder, CO 80301

Circle 172 on reader service card

priced at $35,000 for the 5010 and $40,000 for the 5020.

Analogic Corp., 14 Electronics Ave., Danvers, Mass. 01923. Phone (617) 777-4500 [383]

16-bit analog-to-digital module converts in 7 μs

Zeltex Inc.'s ZAD 7402 analog-to-digital converter provides stable performance and true 16-bit accuracy at a conversion speed of 7 μs. The converter uses the company's "monobit" feed-forward conversion algorithm and is claimed to produce no missing codes over its 0°-to-70°C operating-temperature range.

The ZAD 7402 implements the monobit ladder network, in which equal resistors add or subtract a single unit of current to or from the output as the input code changes incrementally. No switch or resistor can affect a current more than 1/16 of full scale, so the monobit approach is eight times less sensitive to resistor errors than a binary-coded network, where the most significant bit is half of full scale.

The conversion module, which is mechanically configured to drop into existing 16-bit systems, has a 0.4 ppm/°C differential-linearity temperature coefficient, a ±0.0015% accuracy rating, and six-sided electromagnetic and radio-frequency–interference shielding. It requires no adjustments for linearity.

Available four weeks after ordering, each part sells for $895.

Zeltex Inc., 940 Detroit Ave., Concord, Calif. 94518. Phone (415) 686-6660 [384]

Flash C-MOS converter is priced at under $25

A 7-bit complementary-MOS flash analog-to-digital converter that offers programmable power-use levels sells for only $24.95 in lots of 10,000. The TML1073 is fabricated using a high-performance bulk C-MOS process and can operate at a sampling rate of 10 MHz while drawing just 150 mW. If the sampling rate is reduced to 3 MHz, dissipation falls to 50 mW.

Operating current is set at from 20 mA down to less than 0.5 mA by adjusting one external bias resistor, and it is independent of supply voltage. External +3.2- and –3.2-V references are required for operation, and all conversion timing is controlled by an external clock line, which is pulled low when a reading is desired. The digitized analog signal appears at the outputs about 30 ns after the line goes low. After the output data is stored, the clock line can go back to its high state and then another conversion can be requested.

The converter operates from ±5-V supplies in temperatures from –55° to +125°C. Linearity is ±1 least significant bit. In lots of 100, its price is $39.90. Delivery takes two weeks.

Telmos Inc., 740 Kifer Rd., Sunnyvale, Calif. 94086. Phone (408) 732-4882 [385]

Modular system for acquisition, control serves many markets

Operable as a computer peripheral on an IEEE-488 interface bus, the ICE-108A data-acquisition and -control system is accurate to within 0.005%. The unit's analog-to-digital converter runs at 10 samples/s.

Upon scanning, this falls to about 9.7 samples/s. But the actual throughput of a system depends on the speed of execution of the computer's language. For example, a typical low-cost desktop computer running Basic will sample at 5 samples/s, whereas an assembly language program can achieve 9.7.

The system can be configured for applications as varied as process control, research and development, production-line control, and simulation control, thanks to a host of input/output boards. Available to fill the eight slots in the main chassis are programmable resistance outputs, electronic actuator outputs, relay-contact actuator outputs, and digital inputs and outputs, among others.

The main chassis is priced at $4,000. An expander box is available to hold additional boards.

Advanced Technology Research Laboratories Ltd., 5645K General Washington Dr., Alexandria, Va. 22312. Phone (703) 750-2920 [386]

Bit-switching scheme lets converter settle in 400 ns

Thanks to its advanced monolithic bipolar and thin-film–resistor technology, the MC3412 digital-to-analog converter provides stable accuracy characteristics over temperature, along with short settling time. Also, an innovative bit-switching scheme ensures that settling time will be no greater than 400 ns to ±½ least significant bit.

Active laser trimming of thin-film ladder-network, reference, span, bipolar-offset and bandgap-reference resistors at wafer level permit guaranteed limits of gain and offset errors to, respectively, ±0.25% of full-scale range and ±0.05% of full-scale range, without external adjustments. Integral nonlinearity is specified to ±½ LSB of 12 bits with monotonocity guaranteed over the full temperature range.

Precision components in the converter include a 10-V bandgap reference and span and bipolar-offset resistors. With the addition of one external operational amplifier, the span and bipolar-offset resistors can provide calibrated unipolar or bipolar full-scale output voltage ranges of 0 to 5, 0 to 10, ±2.5, ±5, and ±10 V. Available now, the part sells for $17.95; a military version is $63.50.

Motorola Semicondutor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 897-3840 [387]

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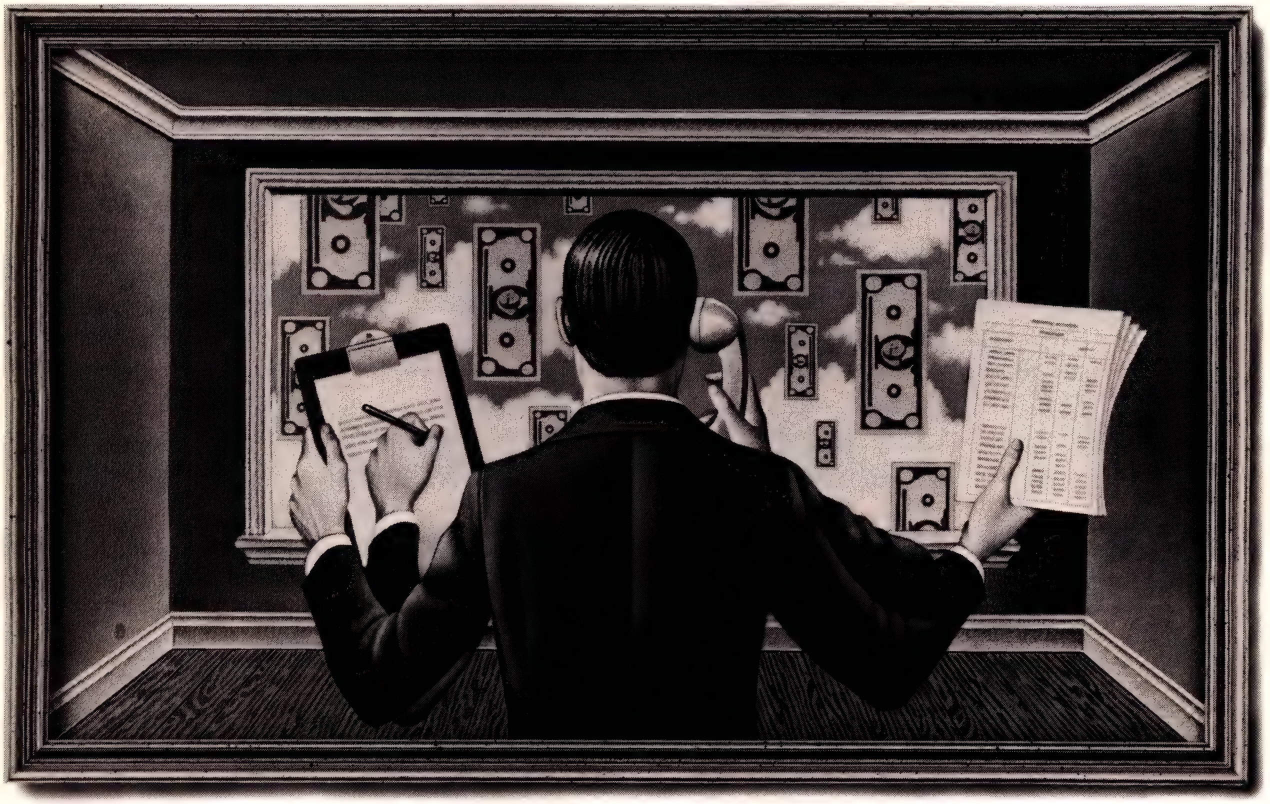

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Circle 176 on reader service card

Communications

IC filters tone from phone line

Chip's bandpass and notch filters detect and suppress 2.6-kHz tone that signals hook-switch condition

A single chip from Motorola Inc. carries a six-pole notch filter and a pair of two-pole bandpass filters for E-and-M (receive and transmit) tone signaling in a central switching office. Based on switched-capacitor filter technology, the MC145432 is intended to reduce the number of components phone companies need in order to generate and detect the 2.6-kHz tone used in hook-switch signaling on phone lines.

Fabricated from Motorola's metal-gate complementary-MOS process, the 140-by-220-mil chip also includes an operational amplifier capable of driving 600-Ω loads. The 18-pin device can operate with either its internal crystal-controlled oscillator or an external clock signal. It may be placed in one of three external-clock modes by tying a pin to one of three system voltage levels.

A 2.6-kHz square wave can be driven into one of the chip's bandpass filters to generate a sine-wave tone of the same frequency. This tone is used to determine the presence of an E-and-M signaling tone on the channel. The other bandpass filter has a Q of 20.

On hook, off hook. In a central office system, the filter chip's bandpass output level is compared with the notch output by external components. If the bandpass channel's output energy level is higher, then a 2.6-kHz tone is present on the incoming line, and the phone is on the hook. When the tone is not found on the incoming line, the phone is off the hook. The notch filter is then used to remove the tone from the outgoing line, so that the phone user does not hear it.

The filter device uses either a split supply of ±5 to ±8 V or a 10-to-16-V single supply. At 10 V, typical power dissipation is 80 mW, and at 15 V, the part uses 200 mW. It has an operating temperature range of –40° to +85°C and TTL– and C-MOS–compatible inputs.

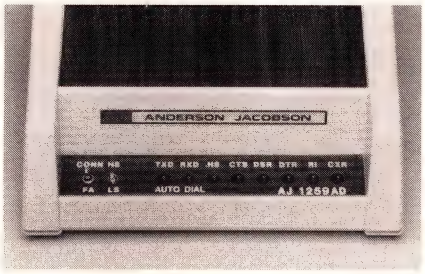
The chip's bypass channel has a maximum idle noise level of 22 dBrnC0, while the six-pole notch filter is listed at 25 dBrnC. At 2.2 and 2.9 kHz, the notch filter's response curve passes through 0 dB, and at 2.6 kHz, through –60 dB.

Available in either plastic or ceramic dual in-line packages, the 145432 is available now in production volumes from Motorola's MOS operation. In 100-piece quantities, the plastic-packaged part sells for $14.49 each, and the ceramic-housed device is priced at $17.06.

Motorola Inc., 3051 Ed Bluestein Blvd., Austin, Texas 78721. Phone (512) 928-6892 [401]

1,200-b/s autodial modem stores 10 phone numbers

A modem with automatic dialing and answering facilities lets users enter, store, and automatically dial up to 10 telephone numbers through simple keyboard commands, in addition to dialing directly from any associated terminal keyboard.



The AJ 1259-AD is a triple modem that is compatible with the Bell 212A and VA 3400 series modems at a 1,200-b/s transmission rate and with the Bell 103/113 modem at 300 b/s. It is approved by the Federal Communications Commission for direct connection to the switched telephone network via RJ-11C modular jacks or RJ-45SD data jacks.

Microprocessor-controlled, the modem offers continuous self-testing and comprehensive diagnostic features. When answering a call, it automatically switches to the appropriate communication protocol and data rate. Available at a price of $875 each, the modems can be shipped in about 30 days.

Anderson Jacobson Inc., 521 Charcot Ave., San Jose, Calif. 95131 [407]

Multiplexer can grow as host system expands

Targeted at computer users who require low-cost multiplexing in systems that have integral expansion capabilities, the DFM series of multiplexers lets users choose among 4, 8, 12, or 16 lines. Expansion to 16 lines from lower line values can be done without uncabling; additional modem cards can be plugged into the DFM backplane.

The multimicroprocessor-controlled DFM multiplexers provide concentration efficiency to 800% and have a 64-K-byte buffer for each group of eight channels. A supervisory channel controls operations and configures data-line priorities for specific applications.

Features of the series include channel switching and contention, error correction, assignable channel priorities, local echo, and channel security, among others. On-board diagnostics enable the multiplexer assembly to provide repair and maintenance information.

To be available in late spring, the multiplexers are priced from $2,800.

Digital Equipment Corp., 29 Parker St., Maynard, Mass. 01754 [403]

Modem rides on board, provides Bell 212A interface

Measuring just 8 in.^{2}, an intelligent component modem dubbed the CH1760 mounts directly onto the host system's printed-circuit board and provides a complete Bell 212A–compatible 300-to-1,200-b/s full-duplex modem; included are telephone-line interface and automatic dialing and answering capabilities registered with the Federal Communications Commission.

The component modem offers a TTL host interface that allows a direct link with virtually any of the popular universal synchronous-asynchronous receiver-transmitters. It is completely controlled by the host that sends it serial asynchronous commands over the serial data lines. Modem speed and parity are automatically set.

Commands include eight diagnostic test modes, voice or data switching, and a data-transparency command called Unlisten that ensures that files or blocks of data can be transmitted through the CH1760 without concern for data being inappropriately interpreted as commands.

Samples sell for $495 each, but in large quantities the price drops to between $200 and $300. The modems are available now.

Cermetek Microelectronics, 1308 Borregas Ave., Sunnyvale, Calif. 94086. Phone (408) 734-8150 [404]

Electronic message processor obeys asynchronous protocols

To become available in the second quarter, the Lettronics 731 electronic-message processor features software protocol selection adaptable to all known asynchronous mail services. The user-definable protocols enable the 731 to switch from one set of parameters to another as communications are established.

No operator intervention is required, enabling the 731 to transfer messages during reduced rate times. Separate log-in procedures, account numbers, passwords, and message format descriptions are identified for each protocol stored.

Designed to work with computers, terminals, word processors, or electronic typewriters, the processor can offload communications tasks to send and receive messages via Telex, TWX, The Source, Compuserve, and Easylink, among others. Delayed transmission, an internal clock-calendar, data and time stamping, and mail-list management, as well as error detection and correction, are standard features; encryption may be specified. The message processor, which has a built-in modem and printer port, will sell for $995 each. Quantity discounts will be available.

Creative Communications Inc., 1662 West 820 North, Provo, Utah 84601. Phone (801) 373-9843 [406]

Fiber-optic data link transmits over 2 km with low error rate

The M25 fiber-optic data link can transmit digital data at rates from dc to at least 25 Mb/s with a bit-error rate of less than 10^{-9}. With a system-wide loss of just 16 dB, transmission lengths of greater than 2 km can be obtained.

As an added feature, the M25 can simultaneously transmit an analog signal up to 10 kHz. Two connector systems are offered: the company's DSC, which is designed to the Electronic Industries Association standards, and the JSC.

The M25 link operates off a 5-V supply and is TTL-compatible. In lots of 100, the link sells for $259. Delivery takes four weeks.

Augat Inc., Interconnection Systems Division, 40 Perry Ave., P. O. Box 1037, Attleboro, Mass. 02703. Phone (617) 222-2202 [408]

Data-encryption device serves networks accessing data bases

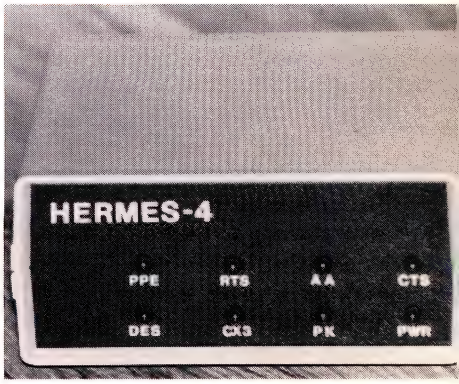
Connected between a computer and remote terminal through its two independently programmable RS-232-C ports, the Hermes-4 data-encryption device adds data privacy to the remote and local networks that currently access a data base in unsecured formats. The device offers users file protection, secure electronic mail, baud-rate translation, protocol handling, program protection, coprocessing, and time-use accounting.

When used as an in-line encryption device, the Hermes-4 may be programmed with any encryption algorithm, including the National Bureau of Standards' Data Encryption Standard, public-key systems, or proprietary encryption algorithms.

As a coprocessor, Hermes-4 can be programmed to do a variety of specific tasks that would otherwise chew up time on the host computer. It is in fact a general-purpose microcomputer with up to 64-K bytes of memory on board in either random-access or read-only configurations. Both RS-232-C ports are programmable and can independently transmit and receive at different baud rates, up to 19.2 kilobaud. Each channel may use 5, 6, 7, or 8 bits per character on receive and transmit as well as 1, 1.5, or 2 stop bits with even or odd parity.

The price, including 2-K bytes of RAM and 4-K bytes of ROM, is $479.

Cryptext Corp., P. O. Box 425, Northgate Station, Seattle, Wa. 98125. Phone (206) 364-8585 [405]



Packaging & production

100-kW lamp anneals wafers

Vortex-stabilized water-cooled argon arc lamp heats wafer to 1,100°C in about 2 seconds

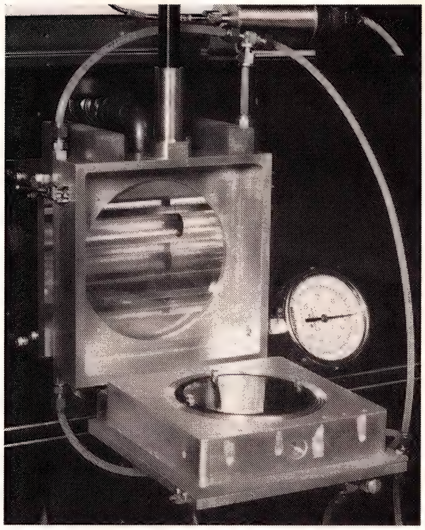
Armed with a 100-kW vortex-stabilized water-cooled dc argon-arc light source that puts out light of such intensity that a wafer can be brought to 1,100°C in about 2 s, the ROA-400 rapid optical annealer from Eaton Corp.'s Ion Beam division is staking its claim as a high-throughput wafer-processing tool for post-implantation wafer annealing and other high-temperature processes.

Because it uses an intense light source for heating wafers at precisely controlled temperatures, the unit can be used to form silicides and alloy contacts, to reflow phosphorosilicate glasses, and to recrystallize amorphous-silicon layers on insulators. In fact, the ROA-400 isothermal processor can be used for almost any standard processing normally done in a wafer furnace.

In addition to the lamp, the equipment consists of wafer-handling, optical, and control systems. Ancillary systems for the lamp include equipment for recirculating and pressurizing the argon gas and deionized water. The user must supply a heat exchanger to cool the water.

Source. The heart of the annealer is the unique lamp head, which forms an arc 11 mm in diameter and 160 mm long. It consists of a quartz tube, the electrode assemblies, and the jets that inject the argon gas and water, which swirl in a vortex down the length of the tube. Both anode and cathode are made of tungsten and are internally cooled to prolong their lives; they can be replaced by the user in 10 to 15 minutes. The tube can also be changed by the user.

The wafer-handling module takes the wafers out of a standard cassette, positions them in the process chamber, removes them for cooling, and then places them in another cassette. The atmosphere surrounding the wafer is controlled during the entire sequence. A shuttle mechanism assures clean, gentle wafer handling at throughputs as high as 360 wafers/h for post-implantation annealing. The system can handle wafers from 3 to 5 in. in diameter.



The ROA-400 will be delivered beginning in the fourth quarter for a price of $250,000.

Eaton Corp., Semiconductor Equipment Operations, 655 River Oaks Parkway, San Jose, Calif. 95134. Phone (408) 942-1555 [391]

Prototype wire-wrapped board for STD-bus goes for $10

Giving designers an inexpensive way of prototyping their STD-bus systems, the wire-wrapped STD-WW1 board is priced at just $10 in single quantities. The board's interleaved power plane makes +5-V power and ground connections simple.

All holes are plated through and are arranged for optimum placement patterns for dual in-line packages. For reliability, gold-plated card-edge connectors are included. Also, hole patterns are arranged at the top of the card for easy placement of header connectors. Delivery takes up to four weeks.

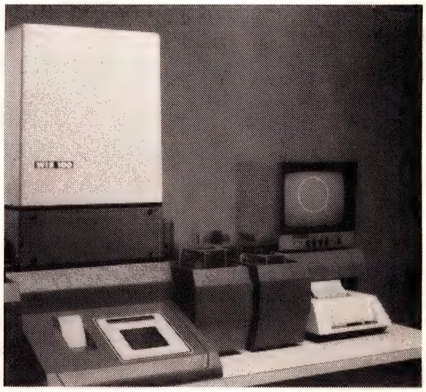
Computer Dynamics, 105 S. Main St., Greer, S. C. 29651. Phone (803) 877-7471 [393]

Laser-based inspectors check 600 silicon wafers an hour

The WIS-100 and WIS-150, two laser-based inspection systems, can process up to 600 silicon wafers an hour, as well as provide data for complete process analysis.

For high-throughput production needs, the stationary WIS-100 offers two input cassettes and automatically sorts into four output cassettes—accept, reject, repolish, or reclean. For spot inspection, the scaled-down WIS-150 fills the bill: it is mounted on wheels for portability.

Based on inspection parameters programmed by the operator, either system will identify over a dozen types of flaws, such as haze, particulates, pits, or mounds. The systems come standard with printers, a cathode-ray-tube terminal, and RS-232-C interfaces. Available in six weeks, the WIS-150 sells for $87,500 and the WIS-100 at $120,000.



Aeronca Electronics Inc., 2940 Interstate St., Charlotte, N. C. 28208. Phone (704) 394-8391 [395]

Eddy-current comparator inspects six parts a second

The Varimac III eddy-current comparator, the smallest and lightest in the company's line, sorts both magnetic and nonmagnetic parts. When used with the firm's sorting gate, it can deal with parts at a rate of six a second. The machine can be used

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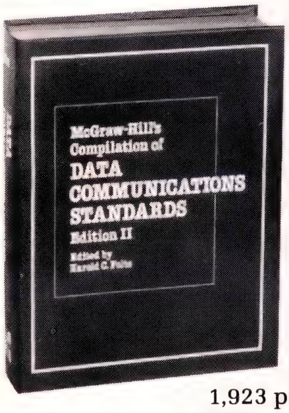
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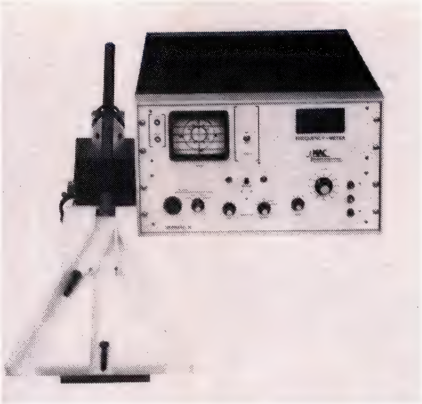

alone or in automated inspection systems where 100% of production must be tested.

The instrument will test for alloy, hardness, case depth, grain size, processing variation, plating thickness, dimension, and orientation. It has a push-button automatic balancing feature that sets it up for a test instantly. The balance circuit can accommodate coils with diameters from under ¼ in. up to 6 in.

A digital readout displays the test-signal frequency, which can be varied from 100 Hz to 1 MHz. The frequency selection, along with 360° phase rotation and a choice of any one of three gate modes on the basis of phase, amplitude, or selected combinations of both, allow optimum separation between significant and insignificant indicators.

The Varimac III is available for sale or lease. With one set of standard coils, it sells for $6,125, and sorting gates go for $1,375 each. The company will design customized systems upon request.

Magnetic Analysis Corp., 535 S. Fourth Ave., Mount Vernon, N.Y. 10550. Phone (914) 699-9450 [394]

Vision system aids in assembly, test, and repair of pc boards

For the assembly, testing, and repair of printed-circuit boards, the model 2200 video image-display system shows correct component placement directly over the board so the operator can see the shape, size, and orientation of components and circuitry to be installed or tested. With specialized software, the system can be expanded in order to perform engineering changes, in-circuit tests, and repairs.

Called the model 2200 circuit-link system, it generates a computerized, step-by-step, graphical representation of the operator's work procedure, increasing speed and reducing the possibility of errors. Consisting of a microcomputer, floppy-disk drive for software, and a projection-monitor work station, the 2200 is suited to small production runs or products with components that cannot be easily adapted to automatic placement.

Options allow versatility in cut and jumper placement, computer-aided repair, in-circuit testing, and incoming inspection testing. Available in 45 days, the 2200 is priced at $25,000.

Electronic Packaging Co., 9995 Monroe Dr., #203, Dallas, Texas 75220. Phone (214) 350-6007 [396]

Programmable cutting system uses laser for reliability

Featuring a 1-kW cutting laser, the Eddco III cutting system can handle complex patterns and a wide variety of materials. Claimed to bring reliable, efficient laser technology to the cutting and machining field, it offers customized table sizes, off-line programming including a digitizer or plotter, a visual display unit with graphics, program storage, and hard-copy capabilities.

The system provides accuracy, repeatability, and product consistency, its maker says, thereby reducing costs for secondary operations, rejects, tooling, and tooling replacements. Accuracy and repeatability are specified as ±0.002 in.

Available optionally is a optical scanning head that can follow an engineering drawing for fast prototype production without the need for programming.

An average system, available in 30 weeks, sells for $325,000.

Printing Techniques International Inc., 43 Vandeventer, Princeton, N.J. 08540 [397]

Sellers of computers will meet their buyers in **Electronics' Special Report: Parallel Architecture**

June 16 issue. Closes May 23.

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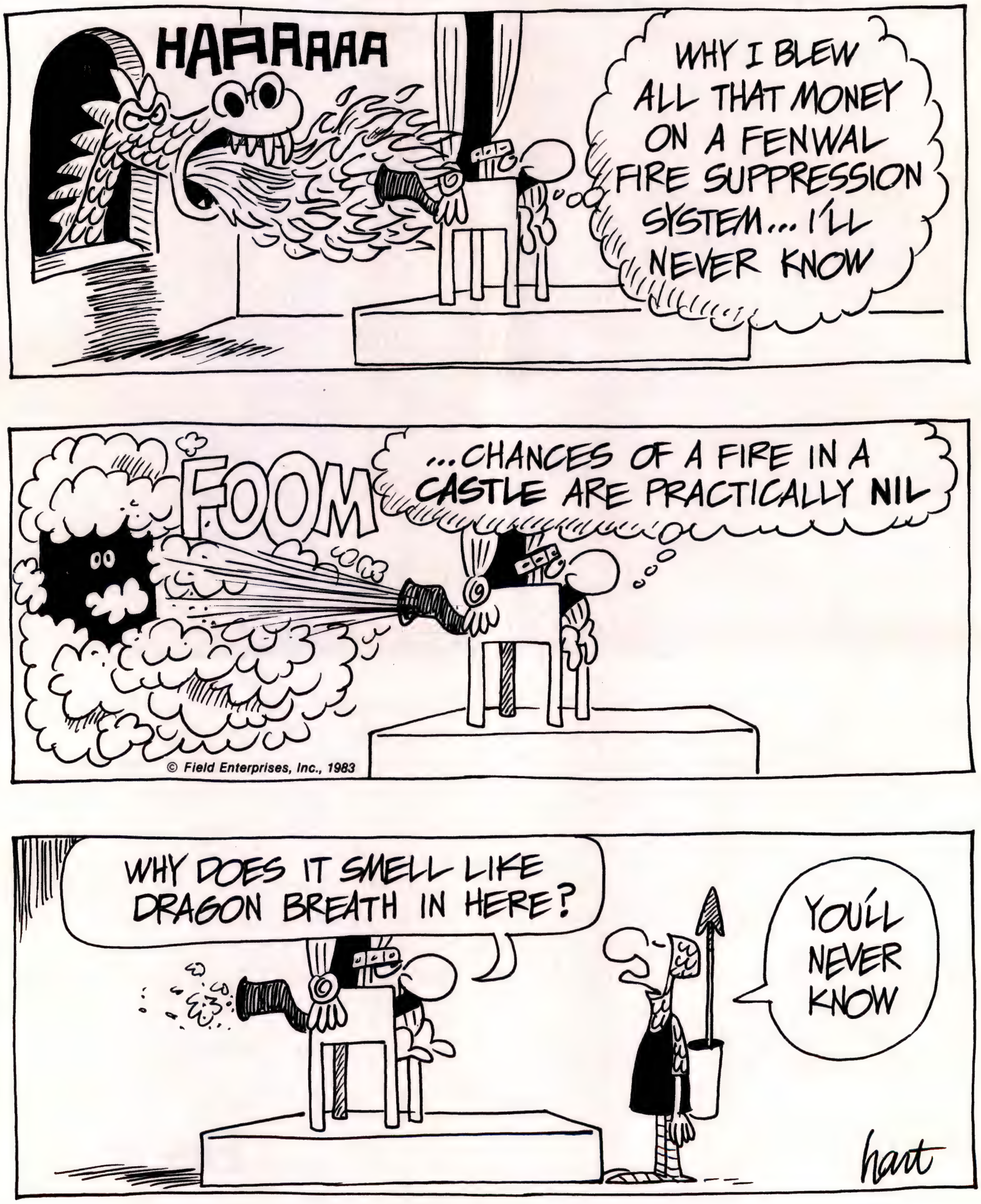
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Products newsletter

Pixel resolution of color-graphics controller hits 1,280 by 1,024

By summer's end, Metheus Corp., a Hillsboro, Ore., maker of graphics products for computer-aided design, will be shipping a color-display controller that boasts a resolution of 1,280 by 1,024 picture elements refreshed at 60 Hz noninterlaced. Called the Ω500, the controller will work with a number of recently introduced 100-MHz video-bandwidth high-resolution color monitors to provide flicker-free displays. A bit-slice microprocessor with a 167-ns cycle time **can draw random vectors at 1.5 million pixels/s and fill rectangles at 35 million pixels/s.** A color look-up table allows over 16 million colors to be displayed on the Ω500, which will be priced at under $20,000.

Application generator runs under Unix, Pick

A new Houston firm, The Software Express, will introduce this month an application generator that produces self-documenting financial and accounting packages to run on supermicrocomputers under the Unix and Pick operating systems. Called Appgen, **the package produces no code, but employs a menu-driven system.** With it, users will enter parameters and system functions that define the way in which basic software modules, provided by Software Express, will be linked for a given application. Either version goes for $15,000.

8-bit microcomputer with E-PROM plummets to $30—for a while

Hoping to attract even a wider range of customers to its complementary-MOS 8-bit microcomputer featuring 2-K of on-chip erasable programmable read-only memory, Motorola Inc. is once again cutting the price. Last month, the company's Austin, Texas, Microprocessor division trimmed the price of the chip—the MC1468705G2—from $250 to $95 for quantities up to 25 [*Electronics,* April 7, p. 56]. Higher yields made the price cut possible, the company said. **Now, effective to the end of September, the operation plans to make a limited offer of up to five devices per application** at a special rate of $30 each. Motorola hopes the offer will encourage budget-limited system designers to consider the use of the microcomputer not only for prototyping but as a production device in equipment that will be produced in low to medium volumes.

Wafer-processing system reduces resist slippage

Slated for introduction at Semicon West next week (May 24–26) is GCA Corp.'s new Wafertrak 1000 wafer-processing system, which includes a module designed to maximize resist adhesion. **The chemical vapor hexamethyldisilazane is dispensed in line to wafers heated to 365°C,** removing all water from the wafer surface prior to resist application. The result, says the Bedford, Mass., equipment maker, is reduced resist slippage and undercutting. A typical system will cost $120,000 and will be available in the third quarter.

Portable computers get colorful

Keep an eye peeled this week at Interface in Boston for Micro Source Inc. to show its portable computers outfitted with NEC Corp.'s **9-in.-diagonal color cathode-ray tube with a resolution of 1,024 by 1,024 picture elements.** For an extra $1,000, the tube can be added to the New Lebanon, Ohio, firm's two Z80A-based 1982 models: the $3,900 dual–floppy-disk M6000P and the $6,395 M6000P/H, which has one floppy and one hard disk.

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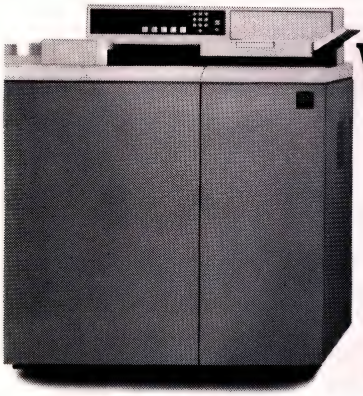

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Career outlook

Another specialty for the EE

In the beginning there was the electrical engineer, the person who designed and built circuits. The world of the EE was populated by such early components as pentodes, triodes, and cat's whiskers; grid currents tickled the fancy and stirred the imagination.

But technology marches on. The bureaucratic side of academia, not known for its speed in adapting to up-to-the-minute techniques and innovations, managed to see some of the handwriting on the wall: a diploma these days most likely will read "electronic engineering."

Now, in the age of the computer, the nation's university engineering departments seem to be trying to emulate industry in their eagerness to subdivide the electronic-engineering curriculum into narrower specialties. Thus, there are EEs, computer scientists, even engineering technologists—and, most recently, the microelectronic engineer.

Inaugurated last fall at Rochester (N. Y.) Institute of Technology, the program now has 55 freshmen and 15 transfer students. "So far as we know, there is no other degree-granting program like it," says a spokesman for RIT, which has a total of 16,000 full- and part-time students. Those 60 will, on satisfactorily completing the five-year sequence, receive bachelors of science in microelectronic engineering.

Eye on processing. The curriculum is heavily practical and focuses on fabrication and processing with an emphasis on photolithography. After a freshman year devoted to basic engineering-style math and physics courses, plus "Introduction to Photoscience for Microelectronic Engineers," the course gets down to business. The next three years bring classes covering semiconductor physics, integrated-circuit technology, circuit analysis, linear systems, optics, digital electronics, microcomputer systems, electromagnetic fields, advanced microlithography, and an IC-processing laboratory.

A recent conference at RIT to mark the program's first year and to fête the seven industry affiliates of the new program (Eastman Kodak, Analog Devices, Fairchild, GCA, IBM, National Semiconductor, and Theta-J) serves as a first-year benchmark. Four papers—three by fifth-year students and one by a graduate who is now at Digital Equipment Corp.—were presented; all had to do with fabrication. The titles of the papers and their authors were:

- "Device Fabrication Using Spin-Dopant Sources," by James Kawski.
- "MOS Operational Amplifier Fabrication," by Juan Becerra.
- "Photoresist Evaluation," by Paulette Farage.
- "The Ability of Surfactants to Assist in the Removal of Image Scum in Positive Resist Development," by Mike Belden.

Like what they see. Representatives of companies at the meeting generally gave the microelectronic-engineering program high grades. Typical is the comment from A. Graham Sterling, vice president for strategic planning at Wilmington, Mass.-based Analog Devices Inc. "The work of the students seemed to me to be very relevant to current industrial needs," he says.

An even more positive reaction comes from Karl Shaw, research assistant at Philips Laboratories in Briarcliff Manor, N. Y., who says, "It's exactly what is needed. There are no such programs [anywhere else] and very few courses in microelectronics. If you're hired as a process engineer, you start out green and it takes at least a year to learn. I feel pretty confident that a graduate from RIT would know what to do right away."

The future seems bright for the program. Plans are already made for a second conference, and, says College of Engineering dean Richard A. Kenyon, the third one might very well be held in a new Center for Microelectronic Engineering that is being considered by the institute. Adds Walt Wojcik, manager of process engineering for IBM Corp. at Hopewell Junction, N. Y.: "I think it's an excellent program. It's certainly going to be well accepted by industry."

–**Howard Wolff**

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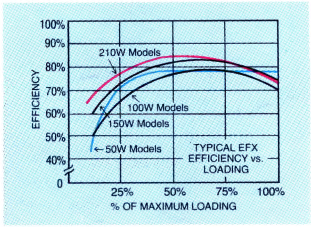

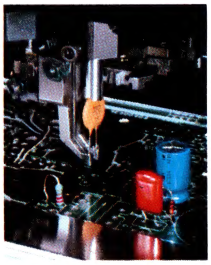

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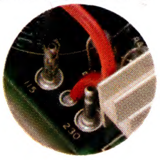
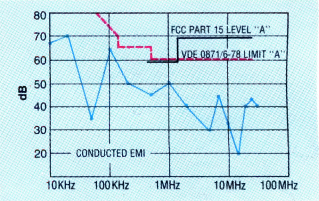
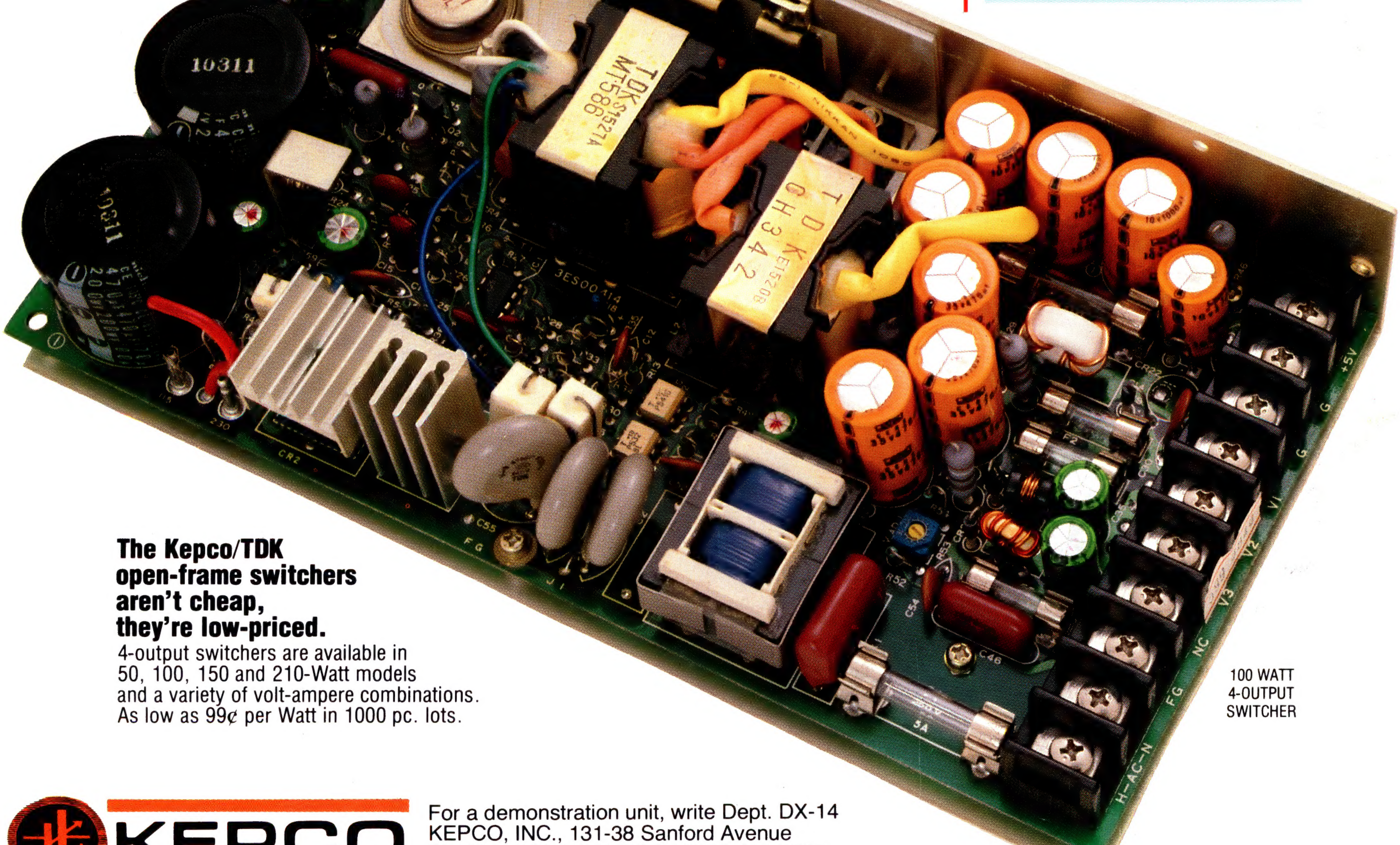


See whether it has an on-board filter. If it doesn't you'll have to add one that meets FCC and VDE requirements. Our conducted noise is not only well under both (see graph), but the on-board filters use special TDK-made VDE-approved capacitors.





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